MICROWAVE-MEASUREMENT-BASED IC INTERCONNECT CHARACTERIZATION, MODELING, AND SIMULATION FOR HIGH SPEED VLSI CIRCUIT DESIGN

By

YUNGSEON EO

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

1993

This dissertation is dedicated to my parents
who have always provided unlimited love and devotion.

ACKNOWLEDGMENTS

I would like to express my deepest gratitude and appreciation to my advisor, Professor William R. Eisenstadt, for his sincere guidance, patient encouragement, and unceasing support in my academic and personal affairs throughout my graduate study. His constructive criticisms and invaluable technical advice made this work possible. It has been a great blessing to me to have been his privileged student. This blessing will remain with me for my whole life.

I am greatly indebted to the Semiconductor Research Corporation for technical and financial support for VLSI circuit interconnect research. In particular, I would like to express my gratitude to the SRC mentors, Dr. Timwah Luk of National Semiconductor, Mr. Hugh Nicolay of Harris, Dr. Quat Vu of Intel, and Dr. Soo Young Oh of Hewlett Packard. They supplied the test structure wafers as well as technical advice for my research.

Dr. Mark E. Law and his students, Mr. Apte Kumar and Mr. Minchang Liang, deserve special thanks for the helpful discussion and advice concerning the PISCES-IIB simulations. Also, I would like to thank Dr. Hanjin Cho for helpful discussion of the scattering parameter measurements. I wish to thank my Ph.D. committee member professors, Drs. William R. Eisenstadt, Shakir A. Abbas, Sheng S. Li, Robert M. Fox, Mark E. Law, and Joseph N. Wilson, who not only read and edited this dissertation, but also participated in my defense and guided my research.

In addition, I would like to thank all of the members of the VLSI TCAD Group of the University of Florida for their helpful discussions and advice.

Also, I would like to express the deepest gratitude to Mr. Gilbert Prost and Mrs. Marian Prost who have given our family great blessing and happiness. I would like to express my gratitude and love to my wife, Young, and my daughter, Ena, for sharing the difficult times of my life. Their endless love and affection have made my life happy and fruitful. Finally, I would like to express to my parents my greatest respect and thanks for their endless love and devotion. Without their sacrifice, it would not have been possible to finish this work. Hence, this dissertation is dedicated to them.

TABLE OF CONTENTS

page

ACKNOWLEDGMENTS iii

ABSTRACT viii

CHAPTERS

1 INTRODUCTION 1

1.1 Introduction to Interconnect Characterization 10
1.2 Introduction to Interconnect Modeling 12
1.3 Introduction to Interconnect Simulation 13

2 REVIEW OF INTERCONNECT ANALYSIS AND MEASUREMENT METHODS 14

2.1 Introduction 14
2.2 Traditional Simulation and Measurement Approaches 16
2.2.1 Full Wave Analysis 16
2.2.2 Quasi-TEM Analysis 17
2.2.3 Use of Simulation Tools 22
2.2.4 Low Frequency Measurements 23
2.3 New IC Interconnect Simulations with PISCES-IIB 24
2.4 Introduction to Scattering Parameters 25
2.5 Time Domain Measurements with TDR and TDT 28
2.6 Suggestion of New Approach 32

3 S-PARAMETER-BASED IC INTERCONNECT TRANSMISSION LINE CHARACTERIZATION 34

3.1 Introduction 34
3.2 Interconnect Characterization 36
3.3 IC Interconnect Transmission Parameter Extraction 41
3.4 Verification of Extraction Algorithm 57
3.5 Y-Parameter De-embedding 60
3.6 Impedance Variation with Frequency 63
3.7 Summary and Discussion 64

4 S-PARAMETER-BASED MULTIPLE TRANSMISSION LINE CHARACTERIZATIONS 65

4.1 Introduction 65
4.2 Mathematical Formulation of Multiline Response 67
4.3 Eigenvalues and Telegrapher's Equation Solution 69
4.4 Propagation Constant and Characteristic Impedance in Two Coupled Lines 74
4.5 Characteristic Impedance Matrix and S-Parameters 77
4.6 Extraction of Coupling Parameters 82
4.7 Test Structure Layout for the Measurements 86
4.8 Summary and Discussion 91

5 HIGH SPEED VLSI INTERCONNECT MODELING BASED ON S-PARAMETER MEASUREMENTS 93

5.1 Introduction 93
5.2 S-Parameter Characterization of Interconnects 94
5.3 Static Interconnect Circuit Parameter Modeling 96
5.3.1 Typical RC-Based Interconnect Models 96
5.3.2 Invariant Parameter RLCG Interconnect Models 100
5.4 Frequency Variant Interconnect Modeling 103
5.4.1 Frequency Variant Resistance Modeling 103
5.4.2 Frequency Dependence of Dielectric Constant 105
5.4.3 Frequency Variant Capacitance and Dielectric Loss 109
5.4.4 Fringing Capacitance 111
5.5 Inductance at High Frequency 119
5.6 Summary and Discussion 124

6 PICO-SECOND SIGNAL TRANSIENT, PROPAGATION, AND CROSSTALK ON LOSSY FREQUENCY VARIANT VLSI INTERCONNECTS 126

6.1 Introduction 124
6.2 Mathematical Formulation of Coupled Interconnects 128
6.3 Line Parameter Matrices for Simulations 133
6.4 Frequency Variant Circuit Parameter Models 134
6.4.1 Diagonal Interconnect Parameters 135
6.4.2 Coupling Capacitance Matrix 136
6.4.3 Coupling Inductance Matrix 144
6.5 Signal Transient, Propagation, and Crosstalk Simulation 145
6.5.1 Simulation Strategy 145
6.5.2 Simulation Models 150
6.5.3 Simulation Results 151
6.6 Experimental Verification in Time Domain 167
6.7 Summary and Discussion 184

7 SUMMARY AND SUGGESTIONS FOR FUTURE STUDY 186

7.1 Summary 186
7.2 Suggestions for Future Study 188

APPENDICES

A S-PARAMETER CALIBRATION OF TWO PORT NETWORKS ... 191

B LOW FREQUENCY CAPACITANCE MEASUREMENTS 200

B.1 Definition of Capacitance 200
B.2 Short Circuit Capacitance and Measurements 203
B.3 Relationship of Various Definitions 207
B.4 Calibration Method (De-embedding) 209

C CIRCUIT RESPONSE OF MULTILINE INTERCONNECT 210

D SKIN EFFECTS IN FINE LINE INTERCONNECT 215

D.1 Skin Effect for a Moderately-Wide Conductor 215
D.2 Estimation of Two Dimensional Skin Depth in Microstrip 217

E ALGORITHMS OF SPAIL 218

E.1 Algorithm: User Interface 218
E.2 Algorithm: Line 220
E.3 Algorithm: Dline 221

REFERENCES 223

BIOGRAPHICAL SKETCH 230

Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

MICROWAVE-MEASUREMENT-BASED IC INTERCONNECT CHARACTERIZATION, MODELING, AND SIMULATION FOR HIGH SPEED VLSI CIRCUIT DESIGN

By

Yungseon Eo

May 1993

Chairman: Dr. William R. Eisenstadt
Major Department: Electrical Engineering

This dissertation presents original research on measuring, modeling, and simulating the performance of Very Large Scale Integrated Circuit (VLSI) interconnects. Novel single line and multiconductor interconnect frequency-domain characterization and modeling and time-domain simulation and verification are presented.

Original IC interconnect test structures were employed for high frequency characterization and modeling. Test structures using advanced BiCMOS process technology are 1 cm by 2, 4, and 10 μm with 2 and 4 μm spacings and using submicron CMOS process technology are 500 μm by 1, 0.8, and 0.6 μm with 1 and 0.8 μm spacings.

New interconnect transmission-line parameter extraction methodologies and pad parasitic calibration techniques demonstrated over 45 MHz to 20 GHz were developed. Single line parameters are extracted from scattering parameter measurements. Coupled line parameters are extracted from single line data and low frequency measurements. Newly

developed software, SPAIL, does automatic interconnect parameter extraction from scattering parameter measurements. Extracted parameters were verified using low frequency capacitance measurements, dc measurements, PISCES-IIB simulations, and HSPICE simulations.

Original frequency variant characterization-based IC interconnect models were developed. These models characterize IC interconnect circuit parameters from fine lines to wide lines and include skin effect, capacitive fringing, and substrate conductance.

A transient simulation algorithm for interconnects was developed using coupled line mathematical analysis and frequency variant parameter models. The algorithm predicts accurate interconnect circuit response for advanced VLSI circuits with new models of pad parasitics. New high speed time domain reflectometry (TDR) and time domain transmission (TDT) measurements in the picosecond range show excellent agreement with simulation.

The dissertation proves that interconnect circuit simulation based on frequency domain characterization and modeling is self-consistent with time domain measurements. These research results can be applied to the timing and signal integrity problems of VLSI circuit design and advanced IC packaging. Signal degradation due to distortion, signal transients, signal delay, and crosstalk noise can be predicted precisely for silicon substrates. These results can be used directly in microwave circuit simulators and work is in progress to use them in SPICE-based simulators.

CHAPTER 1
INTRODUCTION

Today's state of the art VLSI circuits, microwave integrated circuits, and next generation VLSI or ULSI circuit designs face new challenging problems. With the advent of deep submicron semiconductor processing technology, there has been rapid development of IC with integration of more than several million transistors. These VLSI circuits will be operating with clock frequencies greater than several hundred MHz. However, such an increase of integration level and speed raises the risk of poor noise margins and timing malfunctions during circuit operation. Therefore, when designing high performance VLSI circuits, very accurate design methodologies are required.

One of the limiting factors of VLSI circuit designs is interconnect. Without accurate knowledge of interconnect performance, it is impossible to precisely predict during a design stage the clock skew, crosstalk noise, signal delay, and waveform degradation (i.e., signal integrity). Thus, the risk of failure of high performance circuit design increases dramatically.

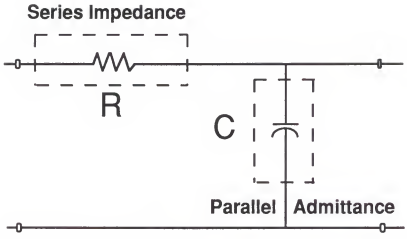
Interconnects have previously been treated as simple conductors modeled with an RC ladder circuit model [Ant83, Sak83]. The conventional RC model have neglected fringing effects, skin effects, and silicon substrate loss. These significantly affect the IC interconnect responses at high frequencies (e.g., propagation delay, rise time, and fall time). Moreover, this RC model predicts inaccurate signal coupling in multiconductor interconnect circuits. Thus, the conventional RC model is

not suitable for circuits that require signal transmission bandwidths over 1 GHz.

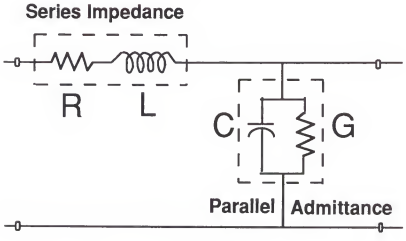
The inaccuracy of the RC model at the high frequencies can be illustrated from the simple comparison of the RC and RLCG interconnect models. Fig. 1-1 shows the distributed circuit model components for single line interconnect modeling. Fig. 1-2 shows the interconnect circuit response for the series impedance and parallel admittance sections of the RC and RLCG models. As seen clearly in Fig. 2-1, these models deviate at about 1 GHz. In order to maintain a sharp controlled edge on a clock it will be necessary to have good model of the clock components up to 5 ~ 10 times the clock frequency [Bog91]. Thus, the RC model will not accurately predict clock edges on the IC in the 100 MHz to 200 MHz regions and beyond. Another rule of thumb relates the bandwidth to a rise time [Gra84],

$$BW = \frac{0.35}{t_{rise}} . \tag{1-1}$$

To accurately model the propagation of 100 ps transmissions on the IC the interconnect models must be accurate to 3.5 GHz. This is clearly not the case for the RC model. Thus, in the near future, microwave characterization techniques and complicated distributed circuit modeling may become necessary for high speed VLSI circuits. This work illustrates the need for distributed circuit modeling in Chapter 3 and introduces a new frequency variant RLCG model for the high speed VLSI circuits in Chapter 5. This model is accurate for transient signals in the 100 ps range. This is demonstrated by measurement in Chapter 6.

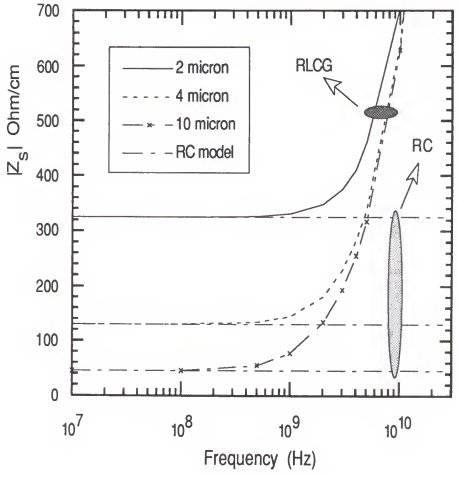


(a)



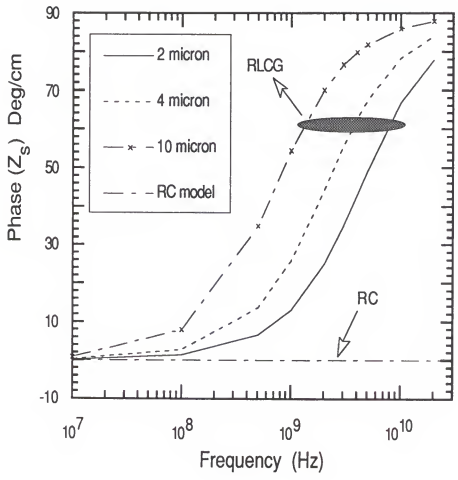
(b)

Fig. 1-1 The Telegrapher's equation equivalent circuit for interconnect transmission lines. (a) RC model used in industry. (b) More accurate RLCG model.

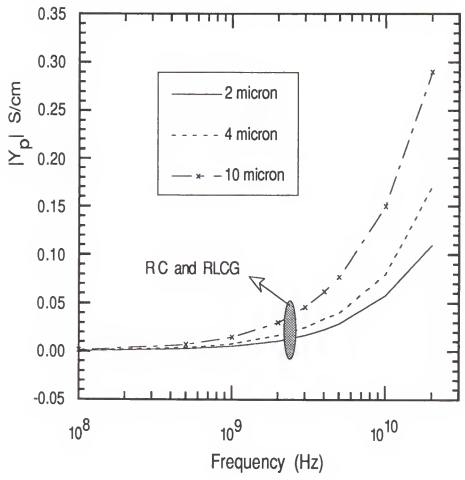


(a) Series impedance magnitude.

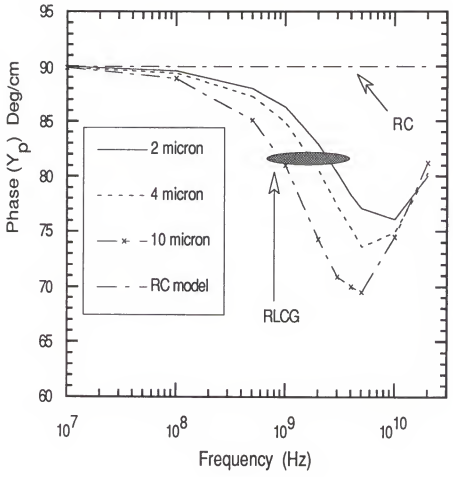
Fig. 1-2 The RC and RLCG (constant parameters except for G) single-line interconnect circuit model response (1 cm long interconnect described in Chapter 3).



(b) Series impedance phase.
Fig. 1-2--continued.



(c) Parallel admittance magnitude.
Fig. 1-2--continued.



(d) Parallel admittance phase.

Fig. 1-2--continued.

This dissertation presents important research on Very Large Scale Integrated Circuit (VLSI) interconnects. This research includes measurement, modeling, and simulation the performance of both single line and multiconductor interconnects on the silicon substrate. Novel interconnect characterization and modeling in the frequency domain and interconnect simulation and verification in the time domain are presented.

Interconnect research can be broken down into three fundamental areas: first, high frequency characterization, second, circuit modeling, and third, time domain simulation. This dissertation considers these three fundamental areas theoretically as well as experimentally.

Original IC interconnect test structures have been built and used for high frequency characterization and modeling. One set of test structures that are 1 cm long, variable widths (2 μm, 4 μm, and 10 μm), and variable line spacings (2 μm and 4 μm) has been designed using advanced BiCMOS process technology of National Semiconductor. Another set of test structures that are 500 μm long, variable widths (1 μm, 0.8 μm, and 0.6 μm), and variable line spacings (1 μm and 0.8 μm) has been designed in a submicron CMOS process technology of Hewlett Packard.

New interconnect transmission line parameter extraction methodologies and pad parasitic calibration techniques for both single line and multiconductor interconnects have been developed in the frequency domain using these new test structures. Single-line Telegrapher's equation parameters are extracted directly from high frequency scattering parameter (s-parameter) measurements. Coupled line parameters are extracted from a combination of single line parameter extraction and traditional low frequency measurements. These results are demonstrated over 45 MHz to 20 GHz. Moreover, the extracted parameters have been

verified using existing methods such as low frequency capacitance measurements, dc measurements, PISCES-IIB (2-dimensional device simulator) simulation, and HSPICE simulation.

New software, Scattering Parameter Analysis of Interconnect Line (SPAIL) [Eo92.b], was created to do automatic interconnect parameter extraction from scattering parameter (s-parameter) measurements. SPAIL is a program composed of FORTRAN-77 code and c-shell script that run on a SUN SPARC workstation under UNIX.

Original frequency variant IC interconnect models based on the characterizations have been developed. These models show for the first time how interconnect circuit parameters vary with frequency. The models provide single and coupled line IC interconnect response. The new models represent fine line interconnect as well as wide line interconnect behavior over a 20 GHz frequency range. They include the skin effect (i.e., skin effect of fine line interconnect) and the effects of capacitive fringing and substrate conductance.

A time domain simulation algorithm for interconnect circuits was developed using exact mathematical analysis of coupled lines and the new frequency variant parameter models. The algorithm predicts accurate interconnect circuit response such as signal transients, propagation, and crosstalk for the advanced VLSI circuit design. Also, models of pad parasitics for time domain simulation have been developed. The validity of the simulation results has been proven by high speed time domain reflectometry (TDR) and time domain transmission (TDT) measurements in the picosecond range. Excellent agreement between simulation results and measurements has been shown. These transient measurements of picosecond coupled lines on the IC are new.

It is shown that interconnect circuit simulation based on frequency domain characterization and modeling is self-consistent with time domain measurements. These research results can be applied to the extremely important timing and signal integrity problems of today's and next century's high performance VLSI circuit design and advanced packaging. Signal degradation due to distortion, signal transients, signal delay, and crosstalk noise can be predicted precisely for silicon substrates using the results of this dissertation. These results can be used directly in microwave circuit simulators and SPICE-based simulators.

This dissertation reviews the literature with the introduction of the basic concepts of high frequency simulation and measurements in Chapter 2. Then, Chapters 3 to 6 present the aforementioned three fundamental areas (interconnect characterization, modeling, and simulation). Finally, Chapter 7 reviews the results and suggests further challenging research areas as well as applications of this research. The ensuing sections of this Chapter introduces the three fundamental areas.

1.1 Introduction to Interconnect Characterization

Currently there are three microwave techniques for semiconductor device characterization: scattering parameter measurements, sampling oscilloscope measurements, and pulsed laser measurements. The scattering parameter (s-parameter) measurement is fundamentally a frequency domain technique, while the remaining two are time domain techniques. The commonly available automated techniques are s-parameter measurements or sampling oscilloscope measurements. The s-parameter and sampling oscilloscope measurement techniques are

reviewed in Chapter 2. Since the pulsed laser measurement technique has been recently developed, it is not readily available, not automated, and not cost effective.

The transmission system characteristics must be related in terms of the measurable quantities to characterize interconnect. Once the relationships between the transmission characteristics and the measurable physical quantities are established, then it is possible to extract the essential transmission parameters directly from experiment. All the other information can be extracted from the transmission parameters.

High frequency characterization requires two important calibrations: equipment calibration and DUT (device under test) parasitic calibration (de-embedding). Equipment calibration can be achieved through standard calibration methods provided by the manufacturer. There has not been a standard method for DUT parasitic calibration for IC interconnect prior to this research (see Chapter 3).

From the calibration point of view, frequency domain characterization is easier and more accurate than time domain. Furthermore, some of the important interconnect transmission parameters can be determined uniquely only by frequency domain characterization. In contrast to the frequency domain techniques, the time domain measurements are widely used to characterize the important circuit design parameters such as delay, crosstalk, or discontinuities. Hence, these two characterization techniques are both very useful in model development and circuit design.

This research uses s-parameter frequency domain characterization for examining interconnect performance. Model verification, however, is

performed with complementary time domain sampling oscilloscope measurements. A new method of extracting interconnect transmission parameters, including DUT calibration, is presented in the Chapter 3 for single interconnect lines and Chapter 4 for coupled interconnect lines.

1.2. Introduction to Interconnect Modeling

While the characterization is used to extract model parameters and electrical characteristics of unknown systems experimentally, modeling is used to find the mathematical or physical expressions to explain and predict future experimental results. Thereby, it is possible through simulations to predict any system's characteristics by combining characterized and modeled components.

Electrical transmission phenomena of interconnect traditionally have been modeled using the Telegrapher's equations. Their model parameters are four coefficient matrices, [R], [L], [C], and [G]. Thus, the four parameter matrices play a pivotal role in accurately predicting the electrical characteristics of interconnects. Ideally, the four model parameter matrices can be determined from semiconductor processing information. This semiconductor processing information includes the physical and electrical description of cross-sectional structures and their physical dimensions.

Chapter 5 presents new modeling of the interconnect parameters in terms of interconnect physical structure. The models are based on s-parameter measurements. Their validity is proved by using existing low frequency measurements and simulation through the numerical device simulator, PISCES-IIB.

1.3. Introduction to Interconnect Simulation

It is essential to simulate targeted circuits by predicting their important electrical design parameters. In complicated modern circuit designs, a circuit without any simulation cannot be iterated upon quickly enough to get a profitable product to market. Simulation results should not only provide the exact electrical characteristics but also suggest design improvements to the circuit designer. Simulation necessarily requires models of the system characteristics and model parameters.

This dissertation integrates IC interconnect characterization with modeling, and presents generalized transient high speed VLSI interconnect simulations. Interconnect circuit characteristics such as very high speed signal pulse, pulse propagation, and crosstalk on modern fine line interconnect are simulated in the time domain. The simulation results are verified with high speed time domain measurements. Chapter 6 of this dissertation describes a novel simulation algorithm including mathematical representation of interconnect circuits and a frequency variant model. Also, existing interconnect models such as constant parameter RC, LC, and RLC model are compared with the new generalized interconnect models.

CHAPTER 2
REVIEW OF INTERCONNECT ANALYSIS AND MEASUREMENT METHODS

2.1 Introduction

As IC interconnect becomes narrower and is integrated in tighter physical configurations, it assumes a pivotal role in high speed circuit performance. Therefore, accurate characterization and modeling of the interconnect will be required in the highest speed circuit designs.

In last several decades, there has been much research concerned with an interconnect transmission line called a microstrip. A microstrip is a metal interconnect line placed on a dielectric substrate of finite width with a ground plane below the substrate. The microstrip has been an essential circuit component in microwave circuits. Microstrip modeling also describes IC interconnect performance at high frequencies.

Although numerous interconnect analysis and design methods have been developed for specific application purposes, their fundamental goals are to calculate characteristic impedance and propagation constant for developing equivalent circuit models. Once characteristic impedance and propagation constant are determined, then all other signal propagation information can be extracted from them.

In this chapter, traditional interconnect characterization approaches are reviewed to give the reader basic background. These traditional methods include full wave analysis, quasi-TEM analysis, and

the use of simulators, and low frequency measurements. These traditional methods are inadequate for advanced VLSI circuit design for the following reasons: 1) they require excessive computation time (e.g., full wave analysis), 2) they require several unrealistic assumptions (i.e., lossless line, zero thickness of interconnect, and constant parameters), 3) they ignore effects of the Si substrate (except PISCES-IIB, a two-dimensional device simulator), 4) most of the analyses only yield capacitance and ignore inductance, resistance, and substrate conductance, 5) all the traditional experimental interconnect characterizations are low frequency techniques, 6) conventional techniques do not take de-embedding of parasitics into account.

With proper treatment, the PISCES-IIB simulation overcomes many of the limitations of the previous methods (e.g., it considers silicon substrate effects, and it does not need intractable analytical formulations and it has reasonable simulation times). In order to explore existing analyses and modeling methodologies and to verify new methodologies, PISCES-IIB simulations of IC interconnect cross sections were done.

High frequency s-parameter and high speed time domain measurement techniques such as TDR (Time Domain Reflectometry) and TDT (Time Domain Transmission) are readily available and realized at the high frequencies. These were used for model development and verification of single and coupled line interconnects in Chapter 3 to Chapter 6.

2.2 Traditional Simulation and Measurement Approaches

2.2.1 Full Wave Analysis

Interconnect (microstrip) full wave analysis requires solving the 3-dimensional electromagnetic (EM) field equations for interconnect geometries. Maxwell's Equations with correct boundary and continuity conditions yield interconnect characteristic impedance and propagation constant. Characteristic impedance and propagation constant are well defined by electromagnetic power which is directly related to EM fields. Thus, for full wave analysis of an arbitrary physical structure, the EM fields must be found given boundary and continuity conditions.

The full wave propagation modes existing on microstrip are described as hybrid in order that all boundary and continuity conditions are satisfied. There are several possible propagation modes on transmission lines. They include transverse electric (TE) mode, transverse magnetic (TM) mode, and transverse electric and magnetic (TEM) mode. Transverse electric or transverse magnetic mode means the magnetic or electric field is perpendicular to the direction of propagation. The idealized (non-hybrid) transverse electric modes, transverse magnetic modes, or transverse electromagnetic modes are only possible by making approximations. That is, there exist longitudinal components of electric field, E, and magnetic field, H, due to the interface between different dielectric materials, boundary conditions, and the transverse components [Gup79]. Time-varying electromagnetic fields must be introduced for the most accurate solution. The full wave hybrid modes may in general be thought of as superpositions of TE and TM fields. The longitudinal and transverse components of EM fields can be represented in terms of scalar

potentials and can be obtained by applying boundary conditions [Gup79]. The full wave propagation analysis yields a pair of coupled integral equations that are solved numerically.

Although the full wave analysis of interconnect is a fundamental approach and may result in accurate answers, the difficulties in its formulation and solving processes restrict it to only simple interconnect structures or to simplified problems. Full wave analysis assumes, in many cases, a lossless system, an absence of transverse currents, and infinitely thin conductors to avoid numerical solutions that take too long. In summary, full wave solutions require numerical analysis with lengthy mathematical derivations and are not practical for interconnect circuit simulation.

2.2.2 Quasi-TEM Analysis

Interconnect (microstrip) may be analyzed and simulated using a simple quasi-TEM based model. Although a real transmission line is not pure TEM, it may be approximated as TEM from the fact that the dominant transmission mode is the TEM mode. This approximated TEM wave is called a quasi-TEM wave. Non-ideal effects such as dispersion can be included in the TEM analysis in order to extend the model bandwidth at high frequencies. Under the quasi-TEM approximation much easier propagation analyses than full wave analysis are available [Djo87]. Furthermore, the analyses may result in closed-form solutions such as those found using conformal mapping techniques. Here, some of the widely used quasi-TEM approaches are reviewed.

Assuming a pure TEM mode, the EM system becomes much simpler. The electric current density (for full wave analysis in which the charge is time varying) is replaced by the charge density in an electrostatic analysis. In full wave analysis, the goal is to obtain the propagation constant and characteristic impedance. The main goal in the quasi-TEM analysis is to find conductor capacitance because most of the necessary information can be determined from this capacitance. Under the quasi-TEM approximation, there are many methods to solve microstrip problems, and yield the capacitance. These are conformal mapping techniques [Hol90], finite difference method (FDM) [Gup79], integral equation methods to solve Poisson's equation (Green's function approaches) [Wee70, Yua83], or variational methods in Fourier transform domain [Yam68].

Since quasi-TEM analysis does not explain non-TEM effects, a dispersion model must be added to the analysis to include these non-ideal effects at high frequencies. That is, dielectric constant and characteristic impedance are modeled as functions of frequency instead of as constants. Thus, with the inclusion of a frequency variant dielectric constant ($\varepsilon_r(\omega)$) model, the accuracy of quasi-TEM analysis at high frequency is improved. The characteristic impedance is varied as a function of the dielectric constant variation. In literature, the many dispersion models are reported [Get73, Pra83].

These quasi-TEM analyses with the dispersion models can accurately predict low frequency capacitance for a lossless substrate but do not predict other transmission parameters. In Chapter 6, it will be shown that LC or RC models based on these analyses are not accurate enough for high performance VLSI circuit design. In LC models the capacitance

comes from quasi-TEM analysis and the inductance is the EM-based inversion of the capacitance matrix, i.e., $LC = \mu_o \varepsilon_o$. Note that this is only valid for a lossless system. In RC models, the capacitance, C, is quasi-TEM-based and the resistance, R, is the measured thin film resistance.

A. Conformal Mapping Techniques [Whe77, Hol90]: Historically, the first microstrip models were constructed by conformal mapping. In many electrostatic quasi-TEM interconnect problems, the potential can be obtained by solving Laplace's equation. Then capacitance is calculated from the Laplace potential. Most of the analytic solutions of Laplace's equation are possible only when variables are separable. Sometimes, nonseparable variables can become separable by transforming coordinate systems. Conformal mapping is a mathematical technique that allows a particular transmission line geometry to be transformed into a new geometry in a second coordinate system [Whe77, Hol90]. A mapping function must be found to transform the coordinate system. The mapping function must be analytic. If the mapping properties are well known, no exploration of the mapping function is required. Otherwise, configurations such as polygonal boundaries (mapping is not clearly indicated) have been obtained through the application of the Schwartz-Christoffel conformal mapping theory [Hol90]. This method guarantees the mapping function to be analytic. Finally, since conformal mapping allows transformation from a nonseparable to a separable coordinate system, it is possible to solve Laplace's equation, i.e., to obtain the equi-potential expression, followed by the capacitance.

Attempts to analyze modern interconnect systems with conformal mapping result in exceedingly complex high order elliptical integration

[Hol90]. Thus, conformal mapping generally assumes pure TEM mode, a lossless system, a thin conductor, and a conductor immersed in homogeneous dielectric to avoid integration difficulties. In summary, conformal mapping yields capacitance in interconnect modeling in a highly restricted set of interconnect geometries. Conformal mapping has strong practical limitations.

B. Use of Green Function [Wee70, Yua83]: The use of Green's function is an alternative technique to find the electrostatic potential of an interconnect system. It permits solutions of interconnect potential that are not possible with conformal mapping. An integral form of Poisson's equation is formulated by a line charge distribution and a Green's function. This is the potential formulated by

$$\phi(r) = \int_D G(r, r') \rho(r') dr' \tag{2-1}$$

where $\phi(r)$ is a potential, $G(r, r')$ is a Green's function, and $\rho(r')$ is a charge distribution. Note, that r is a observation point and r' is a source point. The Green's function can be interpreted as the impulse response or unit source function which is simply the potential due to a line charge of unit charge per unit length. Thus, for an unknown surface charge density, the above integral equation must be solved because all the information except charge distribution is known. The electrostatic potential of the conductor surface is known from boundary conditions and the Green's function of the system is derived from a formulation procedure. This integral equation is usually solved by numerical methods that determine charge or current distribution on conductor surfaces.

In summary, the solution of integral equation method is divided into two processes, i.e., formulation of suitable Green's function for the given system and then solution of the integral equation. Once the integral equation is solved, the charge can be calculated, followed by the capacitance.

Note, it is very difficult to formulate the Green's function and solve integral equations for complicated interconnects (i.e., multilayered system). Also, Green's function analysis is restricted to determining the capacitance for lossless conductor and lossless dielectric interconnect systems.

C. Finite Difference Method and Variational Method: There are two common techniques that model interconnect numerically using a solution of Laplace's equations. Finite Differance Method (FDM) is one of the methods of numerical solution of Laplace's equation [Fra77]. A set of Laplace's equations are written in finite difference form for a net of contiguous equal-sized rectangles into which a transmission line cross section is divided. Then the potentials are determined using the relaxation method. In the relaxation method, the assumed potentials of the first stage of calculation are modified with successive iteration until a specified maximum error is reached. Once the potentials are determined the capacitance can be calculated. FDM is suitable for enclosed microstrip and finite thickness of conductor, but takes a long time for numerical solutions.

The variational Method is the second Laplace-based numerical solution technique [Yam68]. This method obtains upper and lower bounds of transmission parameters in the spectral domain. Analytical treatment of multiple boundaries may be easier using the variational method. In this

method, the variational expression for capacitance with spectral domain potential (which is formulated from Poisson's equation) is represented in the spectral domain. Then the capacitance is numerically calculated. The advantage of this method is there is no need for knowing the charge density distribution accurately and the major portion of the analysis is carried out in the spectral domain.

Note, these techniques also yield only interconnect capacitance for lossless substrates and lossless conductors even after long numerical calculation.

2.2.3 Use of Simulation Tools

There are many commercial and university software packages that extract interconnect parameters or simulate the propagation response of a given system [Djo89a, Djo89b, EEs86, Tma90, Pin85]. The software hide the complicated integral equations or mathematical derivation processes from user. Such software can be used by circuit designers. The software can be categorized into two sets. One set of software is used to perform simple line parameter extraction under quasi-TEM approximations. The other set is employed to perform microwave circuit simulation and optimization such as SUPERCOMPACT, TOUCHSTONE and HP-MDS [Com90, EEs86].

The optimization technique of HARMONICA or HP-MDS is useful for simulating complicated interconnect structures like spiral inductors [Liz92]. These are too complicated for purely theoretical analysis. Thus, industry uses optimized circuit parameter extraction from s-parameter measurement data for this problem. However, this method is not exact, not general, and not predictive.

Optimization techniques have many restrictions but can be applied to IC interconnect measurements. However, they yield little insight into the physical mechanisms governing IC interconnect performance and require a very large array of test data. In contrast, device simulators determine the interconnect parameters more predictively than optimization methods because they solve physical equations of the interconnect cross section without requiring a test device.

However, interconnect simulators (except PISCES-IIB [Pin85, Tma90]) do not consider silicon substrate properties (on which all the on-chip interconnects are fabricated). More detailed PISCES-IIB simulations about IC interconnects are explained in section 2.3.

2.2.4 Low Frequency Measurements

While the analysis and synthesis of overall properties are possible through theoretical approaches, practical problems including nonideal or unexpected effects are found through experiments. Experiments and theory are indispensable to the circuit designer to characterize an unknown system.

In low frequency characterization using open and short circuit measurement techniques, capacitance measurements are easily achieved (see Appendix B, Low Frequency Capacitance Measurements). Capacitance is calculated from the relationship between a short circuit measurement and the definition of capacitance [Wee70]. However, since short and open circuit cannot be easily implemented at high frequencies, other measurement techniques must be used. High frequency

characterization can be accomplished by using scattering parameters (see Section 2.4).

Low frequency capacitance measurements are used to verify new characterization methodologies in Chapter 3 and to characterize multicondutor interconnect in Chapter 4.

2.3 New IC Interconnect Simulations with PISCES-IIB [Eo90]

PISCES-IIB simulations are readily applied to complicated structures such as multilayer interconnect and take into account the silicon substrate properties which vary with frequency and doping concentration. Traditional electromagnetic methods discussed in sections, 2.2.1 and 2.2.2, do not this. Since PISCES-IIB is a 2-dimensional device simulator, it cannot calculate series resistance and series inductance of interconnect, which occur in the third dimension. Nevertheless, it yields interconnect cross sectional information including mutual capacitances and conductance [Eo90]. Since the exact analytical determination of these capacitances and conductance is very difficult, simulation not only is very helpful but also sheds much insight into the capacitance and conductance of IC interconnect on silicon. Furthermore, PISCES-IIB capacitance simulation results agree well with experimental values. Thus, in Chapters, 3, 5, and 6, IC interconnect structures have been simulated with the physical device simulator, PISCES-IIB [Pin85], and capacitance is predicted.

Circuit performance of single line interconnect can be simulated if four line parameters (i.e., R, L, C, and G) are predetermined. PISCES-IIB yields only the capacitance, C, and conductance (dielectric loss), G.

Capacitance is the predominant reactive interconnect parameter at low frequencies. For single line structures on a silicon substrate, simulation results show that as the frequency increases, capacitance values make a transition due to the change of the propagation mode from slow wave mode to quasi-TEM mode [Has71, Has84, Sek84, Eis92]. Analytical calculations show the change of propagation modes in silicon first level metal interconnect is dependent on Si-substrate doping concentration and frequency. On the other hand, the conductance values from both measurements and PISCES-IIB simulations are negligible at low frequencies but substantial at high frequencies.

In multiple conductor interconnect, coupling is encountered during interconnect signal propagation. Capacitive coupling predominates at low frequencies. The coupling capacitances, i.e., mutual capacitances, can be calculated using PISCES-IIB simulations. Because of convergence problems, high frequency effects of mutual capacitance could not be calculated. However, using PISCES-IIB simulation it is possible to estimate high frequency mutual capacitance.

PISCES-IIB simulation gives good insight. However, accurate and rigorous measurements and analytical techniques for extracting all interconnect circuit parameters (capacitance, inductance, resistance, and conductance) are required at moderate and high frequencies.

2.4 Introduction to Scattering Parameters [Hp85, Col66, Fit78]

Scattering parameters (s-parameters) have many advantages over the other network parameters at RF and microwave frequencies. S-parameters are determined with resistive terminations which minimize

parasitic oscillation in active devices, and s-parameters are defined with quantities measurable at high frequencies, i.e., power waves. S-parameter signal flow can be analyzed by using graph theory which makes complex network analysis possible [Fit78]. Scattering parameters are originated from transmission line theory and power parameters. Scattering parameters are related with incident and reflected power, which do not vary in magnitude along lossless transmission lines. S-parameters are used extensively in Chapters 3, 4, 5, and 6.

In contrast, conventional network parameters such as z- (impedance-), y- (admittance-) , and h- (hybrid-) parameters are defined by short and open circuit measurements. These can not be used at high frequency. Magnetically induced inductance in short terminations and electric field fringing in open circuit terminations make the conventional network parameters exceedingly difficult to measure. For active devices, open circuit or short circuit conditions will often result in oscillation [Fit78].

Scattering parameters are defined in terms of traveling waves rather than voltages or currents (unlike other network parameters). First, the incident (V_i^+) and scattered waves (i.e., reflected (V_i^-) or transmitted wave) are defined, followed by s-parameters in terms of these waves [Hp85, Col66, Fit78]. The normalized incident wave is defined as

$$a_i \triangleq \frac{V_i^+}{\sqrt{Z_o}} \tag{2-2}$$

where Z_0 is reference impedance which is commonly 50 Ohms. Likewise, the normalized scattered wave is defined as

$$b_i \triangleq \frac{V_i^-}{\sqrt{Z_o}}. \tag{2-3}$$

Since the square of these waves yields power, the wave "a" is called as power wave entering the device under test (DUT) at a particular port and the wave "b" is called as power wave leaving the DUT. The main reasons for defining s-parameters in this manner are that high-frequency power measurements can be made with relative ease. Then, for the two port network, the scattering parameters are defined as follows,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \triangleq \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{2-4}$$

Thus,

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k = 0,\, k \neq j:\ k = 1,\, 2}. \tag{2-5}$$

The two port scattering parameter can be generalized in the n-port network as follows,

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k = 0,\, k \neq j:\ k = 1,\, 2, \cdots n} \tag{2-6}$$

where $a_k = 0$ means there is no incident signal on the k-th port. The measurement is done in an impedance-matched system.

In reality, good s-parameter measurements cannot be realized without equipment calibration. The DUT is embedded in a measuring system in which microwave components such as transmission lines and connectors are in the signal path from source generator to the DUT. Imperfections of the measuring system cause errors in directivity, frequency tracking, and mismatches. Thus, s-parameter measurements always need calibration to eliminate these errors. Fortunately, such equipment calibration can be routinely performed using standard

calibration methods. The standard network analyzer calibration algorithms are described in Appendix A.

In general, an IC test structure is composed of real DUT and parasitic components such as pads and interconnects. Thus, besides the aforementioned equipment calibration, another calibration called de-embedding has to be performed for accurate high frequency s-parameter measurements. De-embedding eliminates the parasitic components of test device. De-embedding research results will be discussed in Chapter 3 of this dissertation.

2.5 Time Domain Measurements with TDR and TDT

Frequency domain techniques such as s-parameter measurements are an essential part of high speed circuit modeling. While time domain characterization has some similarity to frequency domain characterization, there were no standard techniques to calibrate pad parasitics in the time domain. These pad parasitics are significant in scaled down interconnect measurements [Agr79b, Car69, Tri90].

Nevertheless, most digital circuit model and design parameters such as delay, noise margin, and pulse dispersion are defined in the time domain. Thus, time domain characterizations are an important part of circuit design. Time domain pad calibration is a challenging problem. A new time domain simulation technique for IC pads is presented in Chapter 6.

In high speed circuits, interconnect must be thought of as transmission lines (as in a microwave circuit). TDR and TDT measurements show transmission line discontinuities, signal delay, and crosstalk. TDR characterizes reflected transient signal measurements and

TDT characterizes transmitted transient signal measurements. The reflection coefficient when a signal source with impedance Z_i meets a load impedance Z_j is given by

$$\rho_{ij} = \frac{Z_j - Z_i}{Z_j + Z_i}, \tag{2-9}$$

and the transmission coefficient is given by [Gup81]

$$t_{ij} = \frac{2\sqrt{Z_i Z_j}}{Z_j + Z_i}. \tag{2-10}$$

However, the reflection and transmission coefficient of a lossy transmission line can be obtained only when the transmission line equations (2-11) and (2-12) are solved [Lin90b]. The physical configuration is shown in Fig. 2-1. The transmission line equations of a single line in the frequency domain are

$$V(x,s) = A\,exp(-\gamma x) + B\,exp(\gamma x) \tag{2-11}$$

$$I(x,s) = \frac{1}{Z}\{A\,exp(-\gamma x) - B\,exp(\gamma x)\}. \tag{2-12}$$

Defining the incident wave, reflected (TDR) wave, and transmitted (TDT) waves as follows

$$\begin{cases} V_{incident}(0,s) \triangleq V_i \\ V_{reflected}(0,s) \triangleq V_j \\ V_{transmitted}(l,s) \triangleq V_k \end{cases}, \tag{2-13}$$

the boundary conditions in Fig. 2-1 are given by

$$\begin{cases} V(0,s) = V_i + V_j = A + B \\ I(0,s) = \frac{1}{Z_G}(V_i + V_j) = \frac{1}{Z}(A + B) \end{cases}, \tag{2-14}$$

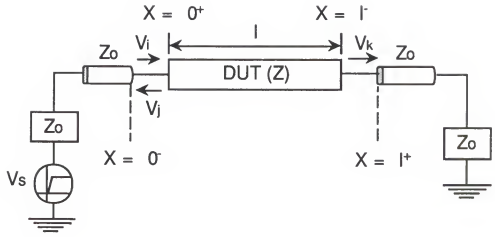


Fig. 2-1 Schematic diagram of TDR and TDT measurements.

$$\begin{cases} V(l,s) = V_k = A\,exp(-\gamma l) + B\,exp(\gamma l) \\ I(l,s) = \dfrac{V_k}{Z_L} = \dfrac{1}{Z}\left(A\,exp(-\gamma l) - B\,exp(\gamma l)\right) \end{cases} . \tag{2-15}$$

Therefore, the reflection and transmission coefficients of the single transmission line are

$$\frac{V_j}{V_i} = \left(\frac{Z}{Z + Z_G}\right)\frac{\rho_G + \rho_L exp(-2\gamma l)}{1 + \rho_G \rho_L exp(-2\gamma l)}, \tag{2-16}$$

$$\frac{V_k}{V_i} = \left(\frac{2Z}{Z + Z_G}\right)\frac{1 + \rho_L}{1 + \rho_G \rho_L exp(-2\gamma l)} exp(-\gamma l), \tag{2-17}$$

where the reflection coefficients of each junction are defined by

$$\rho_G = \frac{Z - Z_G}{Z + Z_G}, \qquad \rho_L = \frac{Z_L - Z}{Z_L + Z}. \tag{2-18}$$

Note, TDR and TDT wave are expressed in terms of interconnect transmission parameters in (2-16) and (2-17). The frequency variant propagation constant and characteristic impedance are given by

$$\gamma(\omega) = \sqrt{(R(\omega) + j\omega L(\omega))(G(\omega) + j\omega C(\omega))} \tag{2-19}$$
$$\triangleq \alpha(\omega) + j\,\beta(\omega)$$

$$Z(\omega) = \sqrt{\frac{(R(\omega) + j\omega L(\omega))}{(G(\omega) + j\omega C(\omega))}} \tag{2-20}$$

where R, L, C and G are interconnect line parameters, i.e., series resistance, series inductance, parallel capacitance, and parallel conductance, respectively, and $\alpha(\omega)$ is attenuation constant and $\beta(\omega)$ is phase constant.

Time domain signals in terms of TDR and TDT can be measured and the measured signal conveys very important information. However,

the propagation constant, $\gamma(\omega)$, and characteristic impedance, $Z(\omega)$, are extremely difficult to extract from a theoretical point of view. The determination of these important parameters is possible from frequency domain interconnect parameter modeling (discussed in Chapter 5).

Both time domain and frequency domain methods are essential for the high performance VLSI circuit modeling. In fact, time domain techniques and frequency domain techniques which are bridged mathematically with Fourier transform or inverse Fourier transform.

2.6 Suggestion of New Approach

As explained in previous sections, traditional modeling and analysis have inherent limitations for today's VLSI interconnect characterization. Thus, a new interconnect characterization methodology is necessary. The techniques (full wave analysis, quasi-TEM analysis, use of existing software, and low frequency measurements) discussed in this Chapter yield interconnect capacitance. From thin film resistance measurements interconnect resistance may be determined. However, a full interconnect parameter set cannot be determined from these traditional methods. Chapter 3 to Chapter 6 show that an frequency variant RLCG model is necessary for high frequency interconnect models (see Chapter 6 for model discrepancies).

S-parameter measurement techniques in the frequency domain and TDR and TDT measurement techniques in the time domain must be used for high speed interconnect characterization. Very important high speed VLSI circuit design parameters such as the signal delay, distortion, clock skew, and crosstalk cannot be exactly predicted from existing

methodologies. Among them, crosstalk is one of the major factors which may cause intermittent circuit errors. Increases in the level of integration lead to increases in average interconnect length as well as much tighter physical configuration. This results in larger coupling capacitance and coupling inductance. Thus, high density and high speed circuits will have more and more serious crosstalk noise as integration levels increase.

More xact interconnect parameter models as well as an experimental extraction methodology for interconnect characterization at high frequency are necessary for high performance circuits and next generation VLSI circuit designs. Simulation techniques in the time domain for very high speed and high density circuits are also necessary because the circuit designer needs accurate interconnect simulation in the time domain.

Hence, the characterizations of high speed and high density IC interconnect must be based on new approaches such as scattering parameter measurements. Then, new high speed VLSI interconnect models must be developed that are simple enough to be used for the CAD subroutines but improve upon conventional models. Finally, the time domain simulation methodology based on new frequency variant models must be developed and verified with time domain experiments.

CHAPTER 3
S-PARAMETER-BASED IC INTERCONNECT TRANSMISSION LINE CHARACTERIZATION

3.1 Introduction

The simplest configuration of interconnect is a single microstrip line on a silicon substrate. Generally, metal interconnect lines in VLSI circuits occupy large amounts of die area and metal lines are multi-layered. Metal layers tend to be orthogonal to simplify design and reduce crosstalk between layers. Furthermore, metal layers will be similar to a solid conductor over a ground plane if spaces are smaller than a wave length of the signal transmitted. Thus, the upper level metal layers tend to be electromagnetically isolated from the substrate by the lower level metal conductors. Therefore, IC interconnect modeling can be divided into first level interconnect with lossy silicon substrate effects and upper level interconnect which is masked from substrate effects.

Early work in first level IC interconnect modeling at microwave frequencies examined microstrip on SiO_2-Si substrates [Has71, Has84, Sek84, Yua91] and three possible modes of signal propagation were described. Interconnect on standard IC substrates exhibits a slow-wave-mode that can be modeled by RC transmission line propagation at low frequencies. As frequency is increased microstrip exhibits a quasi-TEM mode. The previous work extracted impedance and propagation constant for wide interconnect (20 μm to 1600 μm) by measuring short circuit and

open circuit impedances in customized test structures. Standard automated s-parameter techniques were not used for these characterizations.

This dissertation improves upon this earlier work by developing test structure layouts that characterize modern fine line lithography interconnect using standard on-chip microwave probing and s-parameter measurements. Moreover, this study shows how to calculate substrate loss, substrate capacitance, conductor resistance, and conductor inductance of first level and upper level interconnect directly from s-parameter measurements. Strong frequency variations of model parameters are shown, proving that RC modeling of interconnect is fundamentally incorrect at high-frequencies. In addition, basic propagation modes reported in earlier work are verified. Standard automated microwave test equipment can be used by IC designers and engineers to obtain similar results.

In the future, upper level interconnect will have high loss due to small interconnect conductor areas and novel interlayer dielectrics may be used for reduced capacitance [Ush90, Sax92]. Ultimately, it will be necessary for the IC industry to characterize these losses and novel dielectric properties directly from measurement and build a representative interconnect characterization database. From this database, accurate VLSI timing models and interconnect simulators can be developed for the next generation of IC interconnect. This chapter is an important contribution in establishing this experimental database. In addition, the single-line interconnect model presented here is used extensively in the multiconductor interconnect model in Chapter 4 and Chapter 6.

The Chapter is organized as follows. A characterization section reviews test structure design. Then transmission line parameter extraction is reported. Verification of the extraction algorithm using discretized models is presented followed by the discussion of a method to subtract the pad parasitics. Finally, the variation of interconnect impedance with frequency is reported and the study is summarized.

3.2 Interconnect Characterization

Conventional small-signal parameters, *z*-, *y*- and ABCD-parameters, are not suitable for high-frequency interconnect characterizations because open and short circuit terminations required to measure these data cannot be easily realized. "Short" circuit terminations have magnetically induced inductance and "open" circuit terminations have capacitance due to electric field fringing at high-frequencies. On the other hand, s-parameters defined in terms of incident and reflected waves in a controlled 50 Ω measurement system readily characterize interconnect high-frequency response [Dwo79].

In order to perform s-parameter measurements of IC interconnect, a test structure layout was designed as shown on the Fig. 3-1. For example, 4 μm wide and 1 cm long (mask dimensions) Al line over a SiO_2 layer, a thin film nitride layer, and a Si substrate was characterized using s-parameters. The structures were fabricated by National Semiconductor

Other 1 cm long and 2 and 10 μm wide structures on the same test mask fabricated by National Semiconductor were characterized. These National Semiconductor data were used to develope an interconnect line

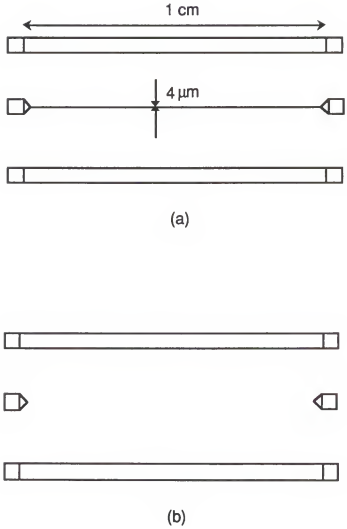


Fig. 3-1 IC interconnect high frequency test structure layout.
(a) test structure layout
(b) open pads of the test structure

parameter extraction algorithm. To solidify the newly developed parameter extraction methodology, other single-line test structures shorter than 1 cm were fabricated by Hewlett Pacard and Harris Semiconductor and were characterized. Through all these test structure characterizations the validity of the extraction algorithm has been proved.

The IC technology cross-section of the test structures is shown on Fig. 3-2. An open structure for the pad calibration was developed that has the same layout as the interconnect test structure without the center conductor. A Cascade Microtech Probe Station and an HP8510 Network Analyzer, which operates from 45 MHz to 20 GHz, measured the interconnect response. The measured data were transmitted to an HP series model 217 computer and ultimately to SUN SPARC workstations for calibration and parameter extraction.

The s-parameter characterization of interconnect transmission is modeled as in Fig. 3-3. Here, a piece of interconnect with characteristic impedance, Z, and propagation constant, γ, is placed in an s-parameter test system of impedance, $Z_0 = 50\ \Omega$. The incident power a_1 and a_2 and reflected power b_1 and b_2 are found and the resulting s-parameter matrix is determined.

Since there are many sources of bad s-parameter data such as external noise, equipment-based microwave resonances, or poor test structure design, very careful experimental technique is essential. Therefore, characterization data met the following criteria. (Otherwise, the data were discarded).

(1) The experimental data from different test structures with identical layout yielded nearly equal values during repeated measurements.

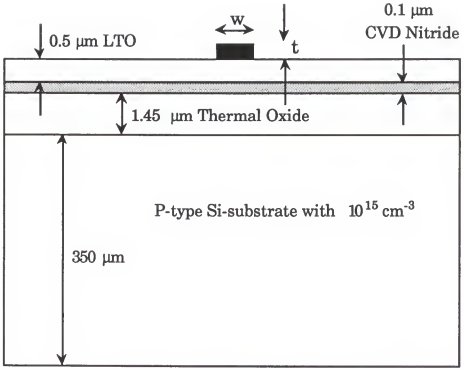
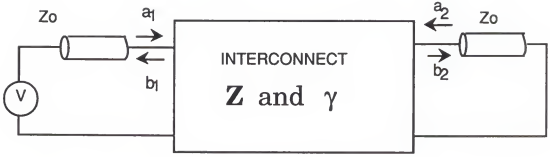


Fig. 3-2 IC interconnect wafer cross-section.



$$[\mathbf{S}] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

Fig. 3-3 S-parameter representation of interconnect transmission.

(2) Since these IC interconnect structures were symmetrical, the s-parameters were symmetrical, $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$.

Interconnect measurements require good equipment calibration as well as consistent elimination of the pad parasitic effects as discussed in section 3.5. Scattering parameters characterizing the above interconnect test structure are shown in Fig. 3-4 (S_{11} and S_{21}). The S_{11} plot on the Smith Chart shows that the imaginary part of the interconnect characteristic impedance is changing from a capacitive reactance to an inductive reactance as the frequency increases. The S_{21} plot shows that the signal transmission becomes increasingly lossy as frequency is increased.

3.3 IC Interconnect Transmission Parameter Extraction

Frequency variations of IC interconnect transmission parameters have been extracted directly from s-parameter measurement data. This information is essential for developing accurate and verified interconnect models. Once these transmission parameters are determined, the interconnect small signal frequency domain response is known and the large time domain response can be obtained by Inverse Fourier transform due to the linearity of interconnect response with voltage.

Interconnect signal transmission is based on the solution of the classical Telegrapher's transmission line equation. A model has been developed that presents, in the frequency domain, single line interconnect voltage and current in terms of propagation constant, γ, and characteristic impedance, Z. Then the impedance and propagation constant are described by four distributed transmission-line parameters, R, L,

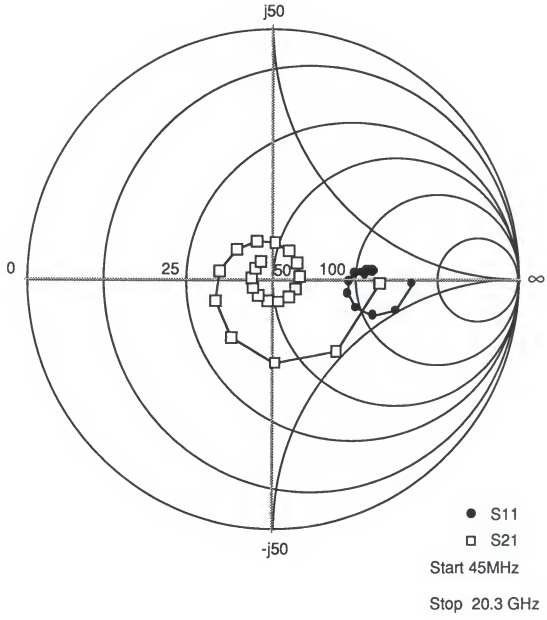


Fig. 3-4 Example s-parameter measurements (S_{11} and S_{21}) of 4 micron wide 1 cm long interconnect.

C, and G. An infinitely small subsection of this model incorporating distributed circuit elements is shown on Fig. 3-5. These distributed circuit parameters describe per-unit-length values and not lumped element values as are assumed in SPICE. In this work, IC interconnect circuit parameters, Z, γ, R, L, C, and G are shown to be functions of frequency. These extracted transmission parameters include pad parasitics. Thus, pad parasitic de-embedding is required. Finally pure interconnect transmission parameters can be determined. To avoid digressing from the main interconnect-parameter-extraction theory, the parasitic de-embedding will be discussed in section 3.5, after transmission-line-parameter extraction and verification.

To solve the Telegrapher's equation for IC-interconnect signal propagation requires an understanding of s-parameter-based interconnect-test-structure characterization. Single line IC interconnect transmission is represented by a two port network and is tested in a controlled ($Z_0 = 50\ \Omega$) impedance microwave measurement system. The s-parameter responses measured from a lossy unmatched transmission line with parameters γ and Z in a Z_0 impedance system are [Gup81],

$$[\mathbf{S}] = \frac{1}{D_s}\begin{bmatrix} (Z^2 - Z_o^2)\sinh\gamma l & 2ZZ_o \\ 2ZZ_o & (Z^2 - Z_o^2)\sinh\gamma l \end{bmatrix} \qquad (3\text{-}1)$$

$$where \quad D_s = 2ZZ_o\cosh\gamma l + (Z^2 + Z_o^2)\sinh\gamma l$$

Since the matrix above is symmetrical, it contains two independent linear equations. This s-parameter matrix is converted to ABCD parameters [Gup81] which incorporate the interconnect propagation

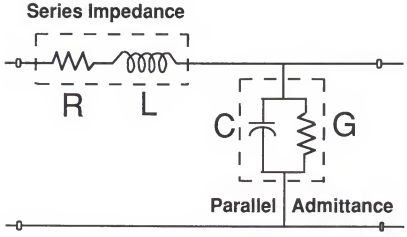


Fig. 3-5 Telegrapher's equation model representation of single conductor interconnect.

constant $\gamma(\omega)$ and the impedance $Z(\omega)$ more explicitly. The equivalent ABCD matrix is,

$$[\,\mathbf{ABCD}\,] = \begin{bmatrix} \cosh\gamma l & Z\sinh\gamma l \\ \dfrac{\sinh\gamma l}{Z} & \cosh\gamma l \end{bmatrix} \tag{3-2}$$

The relationship between s-parameters and ABCD matrix is [Gup81],

$$\begin{aligned} \mathbf{A} &= (1+S_{11}-S_{22}-\Delta S) / (2S_{21}) \\ \mathbf{B} &= (1+S_{11}+S_{22}+\Delta S)\, Z_0 / (2S_{21}) \\ \mathbf{C} &= (1-S_{11}-S_{22}+\Delta S) / (2S_{21}Z_0) \\ \mathbf{D} &= (1-S_{11}+S_{22}-\Delta S) / (2S_{21}) \end{aligned} \tag{3-3}$$

$$\textit{where} \quad \Delta S = S_{11}S_{22} - S_{21}S_{12}$$

The above equations (3-1), (3-2), and (3-3) are combined to yield,

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \tag{3-4}$$

$$\textit{where} \quad K = \left\{ \frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}} \tag{3-5}$$

$$Z^2 = Z_0^2 \, \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \tag{3-6}$$

During the extraction of complex parameters γ and Z from $e^{-\gamma l}$ and Z^2, the cyclically mapped phase output of the s-parameter network analyzer (-180° to +180°) is converted to the true radian measurement

phase which can be any real value. Also, extracted parameters with values that are not physically real, such as negative attenuation constants, must be corrected to be real solutions. Non-physical values satisfy the Telegrapher's equation for propagation in the "negative" direction. Once γ and Z are determined, then from standard transmission line relationships as defined in Chapter 2,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{3-7}$$

$$Z = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{3-8}$$

Then,

$$R = Re\{\gamma Z\} \tag{3-9}$$

$$L = Im\{\gamma Z\}/\omega \tag{3-10}$$

$$G = Re\{\gamma/Z\} \tag{3-11}$$

$$C = Im\{\gamma/Z\}/\omega \tag{3-12}$$

Thus, the Telegrapher's equation transmission line model parameters are determined by combining (3-9) to (3-12).

S-parameter data from the structures described in section 3.2 (see Fig. 3-1 and Fig. 3-2) were used to extract interconnect-line parameters R, L, C, and G. Variations of these four line parameters over 45 MHz to 20 GHz are graphed in Fig. 3-6 through Fig. 3-9. Additional low-frequency test data are included as points "A" and "B" on Fig. 3-6 and Fig. 3-7.

The plot in Fig. 3-6 shows interconnect series resistance increases with frequency owing to the skin effect at high frequencies. The series resistance, which is only determined by physical dimensions of the

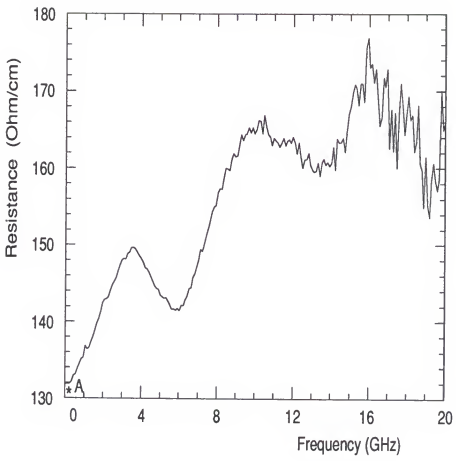


Fig. 3-6 Extracted series resistance/cm versus frequency of 4 micron wide interconnect. A DC measurement that agrees with the extracted 45 MHz data is shown at point A.

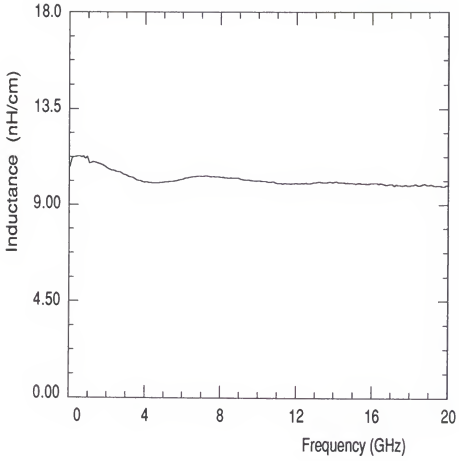


Fig. 3-7 Extracted series inductance/cm versus frequency of 4 micron wide interconnect.

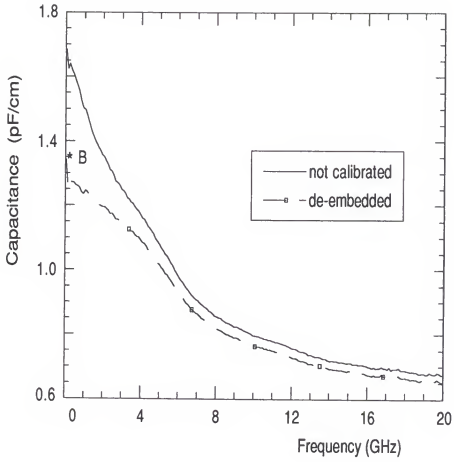


Fig. 3-8 Extracted substrate capacitance/cm versus frequency of 4 micron wide interconnect. A 1 kHz capacitance measurement that agrees with the extracted 45 MHz data is shown at point B.

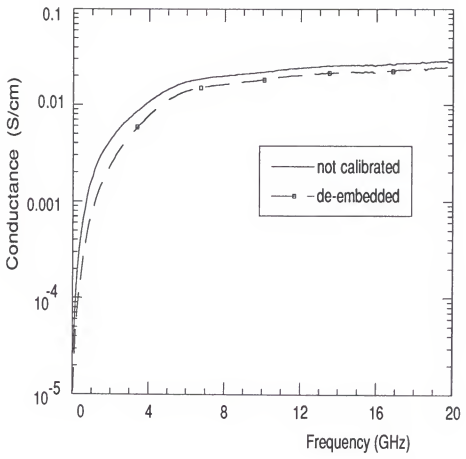


Fig. 3-9 Extracted substrate conductance/cm versus frequency of 4 micron wide interconnect.

interconnect (i.e., conductor width and thickness) at low frequencies, is controlled by both physical dimensions and skin effect at high frequencies. Point A in Fig. 3-6 is the dc series resistance measured with FLUKE 8085A Digital Multimeter through the Cascade Microtech probe station. The dc resistance measurement is 130.3 Ω and the s-parameter-based 45 MHz measured resistance of the 1 cm line interconnect is 131.9 Ω.

The inductance plot in Fig. 3-7 shows that inductance is relatively constant over frequency but does gradually decrease with frequency. However, the reactive effect of a constant value of inductance on signal propagation increases linearly with frequency.

The solid line in Fig. 3-8 shows that interconnect low-frequency substrate capacitance is much larger than the substrate capacitance at high-frequency. The capacitance drops because the interconnect-propagation mode changes from slow wave mode to quasi-TEM mode as frequency increases. Point B in this figure is the interconnect substrate capacitance per unit length measured at 1 kHz by a KEITHLEY 590 CV Analyzer. The 1 kHz interconnect capacitance of 1.36 pF is consistent with the s-parameter-based 45 MHz capacitance of 1.34 pF for 1 cm of interconnect.

Interconnect on a silicon substrate exhibits small dielectric loss at low frequencies that increases monotonically to an asymptote as in Fig. 3-9. Note, this variation is extreme and the conductance scale is a log plot. Some papers in the literature assume that conductive dielectric loss is negligible at all frequencies. However, significant dielectric loss in silicon interconnect is measured at microwave frequencies as shown in Fig. 3-9.

In reality, the conventional RC model can be only used as an approximate interconnect model up to moderate frequencies (discussed in

Chapter 1). A rule of thumb is that interconnect bandwidth must be 5 to 10 times the clock frequency to carry clock signals with sharp edges across ICs [Bog91]. Therefore, single-line interconnect transmission parameters models can have several levels of approximation: first, the constant RC model which is very simple and accurate to several hundred MHz, second, the constant RLC model which can be accurate to frequencies higher than 1 GHz by adding inductive effects, third, the frequency variant RLCG model which is accurate from dc to frequencies greater than 20 GHz.

However, the situation differs in multiconductor interconnects and with coupling between interconnects. The frequency variant RLCG model is superior to all other models when signals are fast enough or spaces are narrow enough to give significant interconnect crosstalk. The accuracy of these models in the time-domain will be discussed in more detail in Chapter 6 using interconnect simulations and measurements.

The transmission line propagation constant and characteristic impedance variations with frequency are shown in Fig. 3-10 through Fig. 3-13. The propagation constant is separated into the attenuation constant (Fig. 3-10) and the phase constant (Fig. 3-11). The attenuation constant increases logarithmically with frequency, and the phase constant linearly increases with frequency. For dc to 1 GHz frequencies the characteristic impedance makes a transition from a very high dc impedance to a constant high-frequency quasi-TEM impedance. The magnitude and the phase of single-line-interconnect characteristic impedance are plotted in Fig. 3-12 and Fig. 3-13, respectively. The magnitude of characteristic impedance is constant over frequencies greater than 1 GHz (Fig. 3-12). The phase of characteristic impedance varies linearly from negative to positive

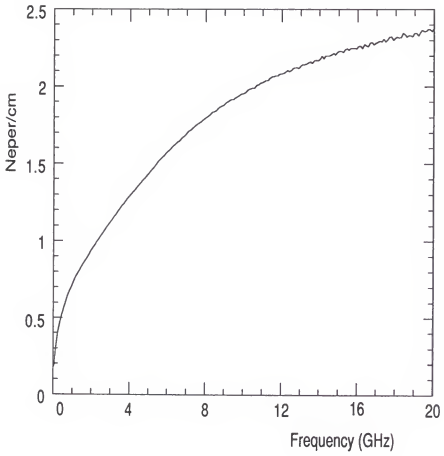


Fig. 3-10 Extracted attenuation/cm versus frequency of 4 micron wide interconnect.

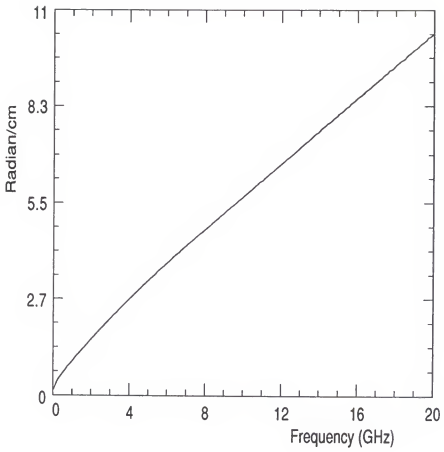


Fig. 3-11 Extracted phase/cm versus frequency of 4 micron wide interconnect.

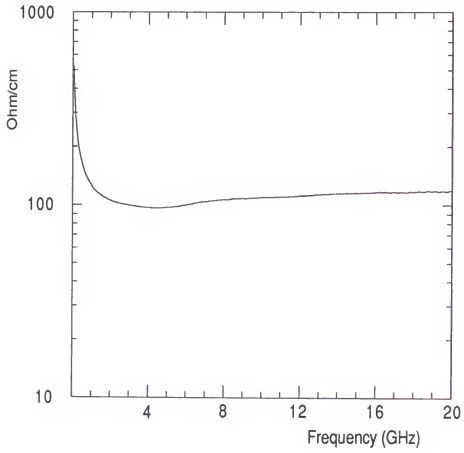


Fig. 3-12 Magnitude of the 4 micron wide interconnect characteristic impedance versus frequency.

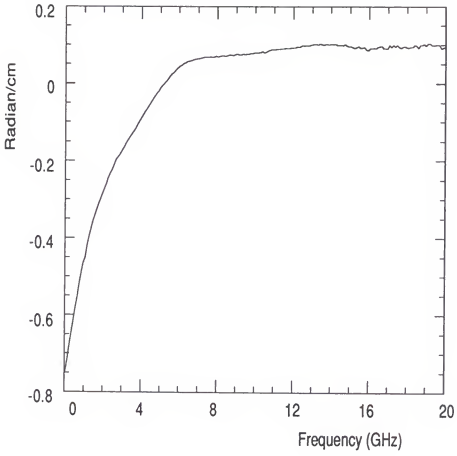


Fig. 3-13 Phase of the 4 micron wide interconnect characteristic impedance versus frequency.

values with increasing frequency and then is fixed at a positive value (0.1 radian/cm) beyond 5 GHz (Fig. 3-13). This phase change from negative to positive values with frequency shows that the transmission line impedance is capacitive at low-frequency and slightly inductive at high-frequency. This is explained in section 3.6.

3.4 Verification of Extraction Algorithm

To verify the newly developed algorithm, the extracted *R, L, C,* and *G,* distributed circuit model was simulated in the frequency domain and s-parameters were calculated using HSPICE [Met91]. The extraction process and verification process are shown in Fig. 3-14. For verification, the distributed circuit transmission model is segmented into a lumped-circuit model representing a 1 cm long interconnect [Ant83]. Here, a ten segment and a hundred segment lumped model were used for simulation. A lumped model, for example, a ten segment model, was built using $R_s = R(\omega) 1\,\text{mm}$, $L_s = L(\omega) 1\,\text{mm}$, $C_p = C(\omega) 1\,\text{mm}$, and $G_p = G(\omega) 1\,\text{mm}$ for each segment. Different segmented models were calculated for six different frequencies. Each segment of the segmented model has the same topology as Fig. 3-5 but uses discrete lumped elements. This approximate verification model permits reversing the process of line parameter extraction from s-parameters.

HSPICE was used to calculate the approximate s-parameter response of these segmented lumped circuit models at the six frequencies. A comparison of the approximate HSPICE results and the measured s-parameters is made in Table 3-1. The ten segment circuit model

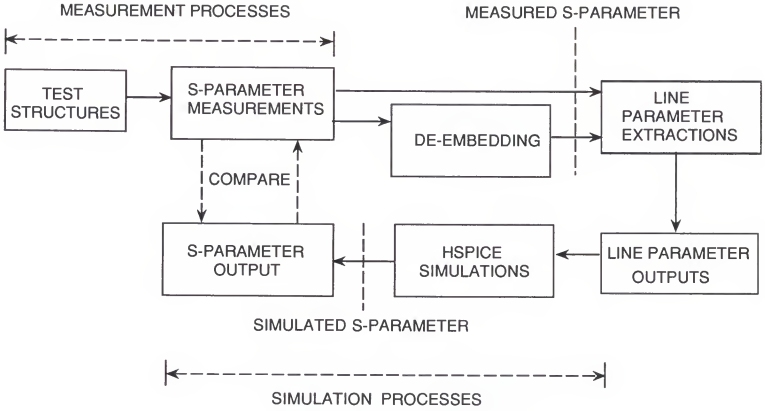


Fig. 3-14 HSPICE verification procedure of the extraction algorithm.

Table 3-1 Comparison of simulated s-parameters with measurement data. The Magnitude (M) of the s-parameters is on a linear scale and the phase (Ph) of the s-parameters is reported in degree.

ITEM	IC line parameters (extracted by using EXTRACTION ALGORITHM)				Measured S-parameters	H-SPICE Simulation (10 segment)	H-SPICE Simulation (100 segment)
Freq. (Hz)	R (ohm/cm)	L (nH/cm)	C (pF/cm)	G (S/cm)	S_{11} M/Ph S_{21} M/Ph	S_{11} M/Ph S_{21} M/Ph	S_{11} M/Ph S_{21} M/Ph
45 M	131.9	10.8	1.7	2.7e-5	.554/-6.6 .420/-2.16	.568/0.00 .430/0.00	.568/0.00 .431/0.00
1 G	136.9	11.0	1.5	1.8e-3	.512/-13.2 .389/-47.9	.516/-9.47 .388/-45.03	.514/-21.1 .388/-45.1
2 G	142.9	10.7	1.4	4.6e-3	.428/-18.6 .337/-88.0	.440/-12.0 .335/-84.65	.433/-17.33 .336/-84.79
5 G	143.5	10.1	1.1	1.4e-2	.305/-.1 .215/173.2	.344/11.44 .209/172.3	.308/1.14 .214/172.6
10 G	165.0	10.1	0.8	2.2e-2	.374/4.3 .121/31.3	.452/18.8 .110/29.0	.380/6.02 .121/33.83
20 G	166.0	9.1	0.7	2.8e-2	.410/5.9 .078/125.6	.560/26.7 .501/105.2	.418/8.68 .077/125.7

approximates magnitude and phase over 5 GHz fairly well. That is, up to 5 GHz, the maximum deviation in magnitude between HSPICE simulation results and measurement data is 12.8% and the maximum phase difference between the two is within 5 degrees. While deviation of the ten segment model becomes larger, as frequency increases, a hundred segment model shows excellent agreement with experimental values at all frequencies. In [Ant83], it was shown in resistive interconnect (RC circuit model) that the ten segment lumped model explains both magnitude and phase. However, it is not adequate for RLCG circuits. As shown in Table 3-1, HSPICE simulation using a hundred segment model shows excellent agreement. These calculations verify the *R, L,* C, and *G* extraction algorithm. Arbitrarily good agreement can be achieved by using an appropriate number of model segments. The model elements R_s, L_s, C_p, and G_p are dependent on frequency so additional modeling work is required to derive the transient signal response. However, the accuracy of alternative model topologies can be investigated using this procedure.

3.5 Y-Parameter De-embedding

In general, pad-parasitic response must be subtracted from test-structure response in high-frequency characterizations. High-frequency de-embedding techniques that eliminate the capacitive effects of pads from the measurement data have been reported [Wij87]. Enhancements in this technique that eliminate series resistances were subsequently proposed by [Cho91]. The series resistance of the pads has a very small effect on IC interconnect extraction. Therefore, the basic y-parameter subtraction method developed by [Wij87] was adapted to interconnect parameter

extraction. Here, the parasitic effects of the pads were modeled as a bond pad capacitance C_b in series with a substrate resistance, R_{sub}. Thus,

$$Y_{\text{pad}} = \frac{(\omega C_b)^2 R_{sub}}{1 + (\omega R_{sub} C_b)^2} + j \frac{\omega C_b}{1 + (\omega R_{sub} C_b)^2} \tag{3-13}$$

$$\equiv G_{pad} + j\,\omega C_{pad}$$

This definition of G_{pad} and C_{pad} models the effects of pad parasitics as a parallel circuit of G_{pad} and C_{pad} in the same topology as IC interconnect substrate C and G are shown in Fig. 3-5. From (3-13), it is evident that pad dielectric loss G_{pad} dominates as frequency increases. The measured test structure data include the effects of these pad parasitics. Thus, with no accounting for parasitic effects,

$$e^{-\gamma} \equiv e^{-(\alpha + j\beta)} = |M| \angle -\theta \tag{3-14}$$

$$\text{where} \quad \gamma = \sqrt{(R + j\,\omega L)(G + j\,\omega C)}\,.$$

After subtracting the effects of pad parasitics,

$$e^{-\gamma'} \equiv e^{-(\alpha' + j\beta')} = |M'| \angle -\theta' \tag{3-15}$$

$$\text{where} \quad \gamma' = \sqrt{(R + j\,\omega L)(G' + j\,\omega C')}\,.$$

Corrected transmission parameters G' and C' without the effects of pad parasitics, can be calculated by characterizing G_{pad} and C_{pad}. Note, $G' = G - G_{pad}$ and $C' = C - C_{pad}$. By squaring (3-7),

$$\alpha^2 - \beta^2 = RG - \omega^2 LC \equiv k_1 \tag{3-16}$$

$$2\alpha\beta = \omega (GL + RC) \equiv k_2. \tag{3-17}$$

Therefore,

$$\alpha = \left\{ \frac{RG - \omega^2 LC}{2} + \frac{1}{4}\sqrt{(RG - \omega^2 LC)^2 + \omega^2 (LG + RC)^2} \right\}^{\frac{1}{2}}$$

$$= \left\{ \frac{k_1 + 0.5\sqrt{k_1^2 + k_2^2}}{2} \right\}^{\frac{1}{2}} \tag{3-18}$$

$$\beta = \frac{\omega (GL + RC)}{2\alpha} = \frac{k_2}{2\alpha}. \tag{3-19}$$

Dividing (3-14) by (3-15), and separating loss and phase terms,

$$\alpha' = \alpha + ln\,(M/M') \tag{3-20}$$

$$\beta' = \beta + \theta' - \theta. \tag{3-21}$$

Therefore, the de-embedded interconnect propagation parameters are,

$$C' = \frac{2\alpha'\beta' R - \omega L(\alpha'^2 - \beta'^2)}{\omega R^2 + \omega^3 L^2} \tag{3-22}$$

$$G' = \frac{R(\alpha'^2 - \beta'^2) + 2\omega L(\alpha'\beta')}{R^2 + \omega^2 L^2}. \tag{3-23}$$

The C' and G' are plotted (dotted line) in Fig. 3-7 and in Fig. 3-9. The capacitance curve in Fig. 3-7 shows the pad parasitic capacitance is much larger at low frequencies and decreases strongly as frequency is increased. The conductance curve in Fig. 3-9 shows pad parasitic loss becomes much larger with increasing frequency.

3.6 Impedance Variation with Frequency

Interconnect characteristic impedance is composed of a real resistive component and imaginary reactive component. A negative interconnect reactance is capacitive and a positive reactance is inductive. This is determined by examining and squaring (3-8),

$$Z^2 = \frac{R + j\omega L}{G + j\omega C}$$

$$= \left(\frac{RG + \omega^2 LC}{G^2 + (\omega C)^2}\right) + j\left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right) \tag{3-24}$$

The real term in (3-24) is always positive and the imaginary term varies from negative to positive with increasing frequency as shown in Fig. 3-13. Considering the imaginary term,

$$if \quad \left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right) < 0, \qquad RC > LG \tag{3-25}$$

$$if \quad \left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right) > 0, \qquad LG > RC \tag{3-26}$$

For the IC interconnect reported in this Chapter the reactive component turns from capacitive to inductive at roughly 5 GHz as shown in Fig. 3-13. In the figure, the phase of the interconnect impedance varies at low-frequency indicating slow-wave-mode propagation while at high-frequencies it is constant and close to 0 radians indicating quasi-TEM propagation. Equations (3-25) and (3-26) show that Neither conductance nor inductance can be neglected in broadband and fast-transient IC interconnect signal propagation.

3.7 Summary and Discussion

A new technique for determining the distributed transmission line parameters from s-parameter measurements of IC interconnect measurement techniques as well as on-chip pad calibration, and algorithm verification are presented. Low-frequency measurements of both series resistance and substrate capacitance confirm the extraction results.

This technique is useful for measuring and extracting interconnect performance of all types of IC interconnect conductors and dielectrics in a single interconnect configuration. From these results approximate limited bandwidth segmented models can be built. The accuracy of the segmented model can be compared to the s-parameter data using the procedure outlined in the extraction algorithm verification section of this paper.

Besides single line parameter extraction which is discussed in this Chapter, coupling parameter extraction is also necessary in order to characterize signal crosstalk in multiple interconnect lines. Signal coupling will be discussed in ensuing Chapter 4.

CHAPTER 4
S-PARAMETER-BASED MULTIPLE TRANSMISSION LINE CHARACTERIZATIONS

4.1 Introduction

Crosstalk noise is a major problem in high speed and high density VLSI circuit designs. This noise is due to electromagnetic coupling between interconnect lines. Crosstalk is becoming very serious as both the circuit speed and the level of integration increases. Crosstalk noise has been explained in the literature using coupled signal analysis. Lossless capacitive coupling is the standard as well as simple way of modeling multiconductor interconnect coupling. However, in the today's scaled down ICs, (whose interconnect is very lossy) inductive, resistive, and conductive effects must be considered as well as capacitive coupling. Thus, the most accurate electrical coupling analysis of multiconductor interconnects requires not only a coupling capacitance matrix but also all other transmission parameter matrices.

Unlike signals on single line interconnect, electrical signal behavior on multiple interconnect lines is best represented in matrix equations. Therefore, proper multiconductor characterization implies accurate mathematical representation of interconnect response and model parameter extraction using this representation. The development of 1) the mathematical formulation representing multiline interconnect circuits, 2) the representation of multiline interconnect characteristic impedance by

microwave circuit parameters, 3) the development of an efficient approximate coupled line parameter extraction and, 4) multiconductor interconnect test structure development are the crucial results of this chapter. The mathematical formulation representing multiconductor interconnect circuit impedance and propagation constants is a comprehensive assembly of results reported in the literature. The efficient approximate coupled line parameter extraction methodology and multiconcuctor interconnect test structure developments are new research results.

The mathematical modeling of a multiconductor system is represented by an n-dimensional extension of the Telegrapher's equation. Then multiconductor system parameters such as the propagation constant matrix and the characteristic impedance matrix can be obtained theoretically in terms of transmission-line-parameter matrices by using matrix analysis. These theoretical analyses provide physical understanding of interconnect circuits and show that direct extraction of coupled interconnect parameters is exceedingly difficult.

A new simplified coupling parameter extraction methodology that combines single line s-parameter measurements, low frequency coupling capacitance measurements, and the solution of coupled interconnect matrix equations is presented. A key part of the method is the development of a new expression for the self capacitance of coupled lines. The validity of the method will be proved with high speed time domain measurements in Chapter 6. Novel multiconductor interconnect test structures have been developed in the HP25 submicron CMOS technology. These are 0.5 mm long and have submicron widths and spaces. They were used to prove

experimentally the new self-capacitance expression developed for coupled lines.

The chapter is organized as follows. The mathematical formulation of multiconductor interconnect signal propagation and its solution are presented. Then the relationships between the mathematical model parameters such as propagation constant and characteristic impedance are described in terms of line parameter matrices. Finally, efficient approximate parameter extraction method and test structure layouts are presented.

4.2 Mathematical Formulation of Multiline Response

The mathematical formulation of multiconductor interconnect response is performed using the Telegrapher's equation. Electrical properties of multiconductor lines can be represented by the following matrix form of the Telegrapher's equations [You90, Ghi89, Djo87],

$$\frac{d[V(x)]}{dx} = [Z_s][I(x)] \tag{4-1}$$

$$\frac{d[I(x)]}{dx} = [Y_p][V(x)] \tag{4-2}$$

where $[V(x)]$ and $[I(x)]$ are line voltages and currents and $[Z_s]$ and $[Y_p]$ are composed of

$$[Z_s] = [R] + j\omega[L] \tag{4-3}$$

$$[Y_p] = [G] + j\omega[C] \tag{4-4}$$

where $C_{ii} = \sum_{j=1}^{n} c_{ij}$ *and* $C_{ij} = -c_{ij}$,

$$\textit{similarly} \quad G_{ii} = \sum_{j=1}^{n} g_{ij} \qquad \textit{and} \qquad G_{ij} = -g_{ij} \ .$$

Here, $[C]$ is the short circuit capacitance matrix and can be expressed in terms of capacitance (c_{ij}). This is discussed extensively in Appendix B. By combining (4-1) and (4-2),

$$\begin{aligned} \frac{d^2[V(x)]}{dx^2} &= [Z_s][Y_p][V(x)] \\ &= \gamma^2 [V(x)] \ . \end{aligned} \tag{4-5}$$

The solution of m-th eigenmode has the form of

$$\begin{cases} [V_m(x)] = [V_m(0)]\, exp(\pm\gamma_m x) \\ [I_m(x)] = [I_m(0)]\, exp(\pm\gamma_m x) \end{cases} \qquad \textit{for m-th eigenmode, } \gamma_m \tag{4-6}$$

considering the following differential equation

$$\begin{aligned} \frac{d^2V}{dx^2} &= Z_s Y_p V \\ &= \gamma^2 V \end{aligned}$$

whose solution is

$$V = V(0) exp(\pm\gamma x) \ .$$

Thus, plugging (4-6) into (4-5),

$$\left\{\gamma_m^2 [U] - [Z_s][Y_p]\right\}[V_m(0)] = 0 \tag{4-7}$$

where $[U]$ is identity matrix. For (4-7) to have non-trivial solutions, the corresponding eigenvalue problem must be satisfied by

$$det\left\{ \gamma_m^2 [U] - [Z_s][Y_p] \right\} = 0 \ . \tag{4-8}$$

Equation (4-8) is the basis of the solution of multiconductor interconnect lines. Matrices $[Z_s]$ and $[Y_p]$ are provided by the physical properties of the multiconductor interconnect. The solution for γ_m^2 provides the m-th eigenvalue of the matrix $[Z_s][Y_p]$. These eigenvalues lead to the propagation constants and characteristic impedances of the interconnect. The propagation constant and characteristic impedances are used to calculate interconnect circuit wave modes, propagation speed, and attenuation. This will be discussed below.

4.3 Eigenvalues and Telegrapher's Equation Solution

The mathematical requirements for eigenvalue solution of (4-8) is the condition that (4-8) matrix system equation has non-trivial solutions, but the physical meaning of the solution requires some interpretation.

The response of the interconnect system is represented by matrix equations as a linear combination of eigenvectors which are solutions corresponding to each eigenvalue. In other words, the solution of the interconnect propagation is represented as the linear combination of each solution vector with unknown constants. These unknown constants must be determined from external conditions such as boundary conditions or physical properties of the system. Thus, the calculation of the interconnect matrix eigenvalue is the most crucial part as well as the first step of the interconnect matrix analysis. The eigenvalue calculation is followed by the solution of the interconnect matrix linear system. Likewise, only if boundary conditions and eigenvalues are known in the interconnect system, can changes of the voltage and current waveforms on the conductors be predicted. For the m-th eigenmode,

$$\left\{\gamma_m^2[U] - [Z_s][Y_p]\right\}[V_m(0)] = 0 . \tag{4-9}$$

The eigenvalues of matrix equation (4-9) are solved in Appendix C. Representing solution vectors as a matrix form, the interconnect voltage

$$[V(x)] = [S_v][E(x)][C_1] + [S_v][E(x)]^{-1}[C_2] \tag{4-10}$$

where $[S_v]$ is the $n \times n$ voltage eigenmatrix, $[E(x)]$ is diag$\{e^{-\gamma_1 x}, \cdots, e^{-\gamma_n x}\}$, and $[C_1]$ and $[C_2]$ are constant column vectors. Likewise, plugging (4-10) into (4-1), the current equation becomes

$$[I(x)] = [S_i][E(x)][C_1] - [S_i][E(x)]^{-1}[C_2] \tag{4-11}$$

$$\textit{where} \quad [S_i] = [Z_s]^{-1}[S_v]\,[\Lambda] \tag{4-12}$$

where $[S_i]$ is the $n \times n$ current eigenmatrix and $[\Lambda]$ is diag$\{\gamma_1, \cdots, \gamma_n\}$. Combining the terminal network with an interconnect network as in Fig. 4-1,

$$[E_i] = [V(0)] - [Z_G][I(0)], \tag{4-13}$$

$$[V(D)] = [Z_L][I(D)]. \tag{4-14}$$

Inserting (4-10) and (4-11) at x = 0, (4-13) becomes

$$[E_i] = [S_v][E(0)][C_1] + [S_v][E(0)]^{-1}[C_2] + [Z_G]\left\{[S_i][E(0)][C_1] - [S_i][E(0)]^{-1}[C_2]\right\}. \tag{4-15}$$

Since [E(0)] and $[E(0)]^{-1}$ are identity matrices, (4-15) is represented as

$$[E_i] = \{[S_v] + [Z_G][S_i]\}[C_1] + \{[S_v] - [Z_G][S_i]\}[C_2]$$

$$= \begin{bmatrix} [S_v] + [Z_G][S_i] & [S_v] - [Z_G][S_i] \end{bmatrix} \begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix}. \tag{4-16}$$

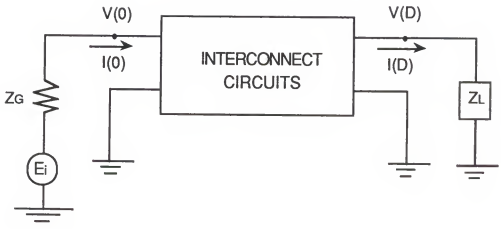


Fig. 4-1 Two port network with load impedance.

Similarly, (4-14) becomes

$$
\begin{aligned}
[0] &= [V(D)] - [Z_L][I(D)] \\
&= [S_v][E(D)][C_1] - [S_v][E(D)]^{-1}[C_2] + [Z_L]\{[S_i][E(D)][C_1] - [S_i][E(D)]^{-1}[C_2]\} \\
&= \{[S_v][E(D)] + [Z_G][S_i][E(D)]\}[C_1] - \{[S_v][E(D)]^{-1} - [Z_G][S_i][E(D)]^{-1}\}[C_2] \\
&= \begin{bmatrix} ([S_v] + [Z_L][S_i])[E(D)] & ([S_v] - [Z_L][S_i])[E(D)]^{-1} \end{bmatrix} \begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix}. \qquad (4\text{-}17)
\end{aligned}
$$

Finally, (4-16) and (4-17) can be combined to the following matrix form

$$
\begin{bmatrix} [E_i] \\ [0] \end{bmatrix} = \begin{bmatrix} [S_v] + [Z_G][S_i] & [S_v] - [Z_L][S_i] \\ ([S_v] + [Z_L][S_i])[E(D)] & ([S_v] - [Z_L][S_i])[E(D)]^{-1} \end{bmatrix} \begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix}. \qquad (4\text{-}18)
$$

Equation (4-18) is important because it relates multiconductor interconnect propagation to fundamental physical properties of the interconnect, load, and generator. This equation has not been explicitly derived in the literature but occasionally is used. The constant vectors $[C_1]$ and $[C_2]$ which are determined from the boundary conditions are magnitudes and phase of the incident and reflected waves. Equation (4-18) represents signal variations on multiconductor circuits mathematically. That is, if the voltage eigenmatrix, the current eigenmatrix, and the boundary conditions are known, interconnect circuit response can be completely determined. Note, eigenmatrices can be represented in terms of four interconnect circuit parameter matrices. Thus, the determination of interconnect parameter matrices is fundamental as well as important work.

Under assumption that $Z_{G1} = Z_{G2}$ and $Z_{L1} = Z_{L2}$ and interconnect circuit parameters are constant, the solution of the equations for two coupled lines becomes the interconnect circuit transfer function [You90, Hwa91],

$$H_1 = \frac{1}{2}(T_1 + T_2) \tag{4-19}$$

$$H_2 = \frac{1}{2}(T_1 - T_2) \tag{4-20}$$

where

$$T_1 = \frac{Z_1}{Z_1 + Z_G} \frac{exp(-\gamma_1 x) + \rho_{L1} exp(-\gamma_1(2l - x))}{1 - \rho_{G1}\rho_{L1} exp(-2\gamma_1 l)},$$

$$T_2 = \frac{Z_2}{Z_2 + Z_G} \frac{exp(-\gamma_2 x) + \rho_{L2} exp(-\gamma_2(2l - x))}{1 - \rho_{G2}\rho_{L2} exp(-2\gamma_2 l)},$$

where

$$\rho_{L1} = \frac{Z_L - Z_1}{Z_L + Z_1}, \quad \rho_{G1} = \frac{Z_G - Z_1}{Z_G + Z_1}, \quad \rho_{L2} = \frac{Z_L - Z_2}{Z_L + Z_2}, \quad and \quad \rho_{G2} = \frac{Z_G - Z_2}{Z_G + Z_2}.$$

The above equations (4-19) and (4-20) are widely used as accurate transfer functions and are a direct simplification of (4-18). With further assumptions, they can be represented in closed form in the time domain. Moreover, if impedance matching conditions are satisfied, then a simpler form is produced [Veg86, Whi91, Cur85],

$$T_i = 0.5exp(-\gamma_i x). \tag{4-21}$$

Although the above expression (4-21) is useful for high speed VLSI circuit designs as a simplified form of the interconnect transfer function, it has many application at low frequencies or in carefully designed microwave

circuits with matched generator and load resistances. A new more generalized transfer function for frequency variant interconnect parameters and unequal impedance terminations will be developed in Chapter 6.

4.4 Propagation Constant and Characteristic Impedance in Two Coupled Lines

In the multiconductor interconnect system, electrical signals are physically represented in terms of propagation constants but mathematically represented in terms of eigenmatrices. Namely, eigenvalues in mathematical analysis are physically associated with propagation constants in multiconductor circuits. Thus, their relationship should be reviewed.

Below, propagation constants are given in terms of eigenvalues. Then, characteristic impedance is defined in terms of eigenmatrices and again related to interconnect line parameter matrices.

For two coupled lines, propagation constants can be derived by using matrix analysis, i.e.,

$$\left(\gamma^2[U]-[Z_S][Y_P]\right)[S_v]=0 \tag{4-22}$$

where $[U]$ is the identity matrix and $[S_v]$ is the voltage eigenmatrix. To have a non-trivial solution, (4-22) must satisfy

$$\left|\gamma^2[U]-[Z_s][Y_p]\right|=0 \,. \tag{4-23}$$

Letting

$$[Z_s][Y_p] \triangleq [A] = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

$$\gamma^2 \triangleq \lambda .$$

The characteristic equation for two coupled lines becomes

$$\begin{vmatrix} \lambda_1 - A_{11} & -A_{12} \\ -A_{21} & \lambda_2 - A_{22} \end{vmatrix} = 0 . \tag{4-24}$$

Therefore, assuming symmetrical structures (i.e., $A_{11} = A_{22}$ and $A_{12} = A_{21}$) the eigenvalues for two coupled lines are as follows

$$\lambda_1 = A_{11} + A_{12} \tag{4-25}$$

$$\lambda_2 = A_{11} - A_{12} . \tag{4-26}$$

These result in,

$$\lambda_1 = \gamma_1^2 \qquad \therefore \ \gamma_1 = \pm\sqrt{(Y_{11} + Y_{12})(Z_{11} + Z_{12})} \tag{4-27}$$

$$\lambda_2 = \gamma_2^2 \qquad \therefore \ \gamma_2 = \pm\sqrt{(Y_{11} - Y_{12})(Z_{11} - Z_{12})} \tag{4-28}$$

where γ_1 and γ_2 are propagation constants of the eigenmodes.

The characteristic impedance matrix can be defined in terms of a voltage eigenmatrix and a current eigenmatrix from matrix analysis. In more detail, the left most terms after the equal sign of both (4-10) and (4-11) are incident waves and the second terms are reflected waves. Thus, from the characteristic impedance definition, which is the incident voltage wave divided by the incident current wave,

$$[Z_c] = [S_v][S_i]^{-1} . \tag{4-29}$$

The voltage eigenmatrix in (4-29) can be obtained by finding eigenvectors corresponding to eigenvalues, λ_1, and λ_2. In other words, λ_1 and λ_2 are inserted for γ_m in (4-9).

$$\{\lambda_1[U]-[Z_s][Y_p]\}[S_1]=0 \tag{4-30}$$

$$\{\lambda_2[U]-[Z_s][Y_p]\}[S_2]=0\,. \tag{4-31}$$

Plugging (4-25) into (4-30),

$$\left\{\begin{bmatrix} A_{11}+A_{12} & 0 \\ 0 & A_{11}+A_{12}\end{bmatrix}-\begin{bmatrix} A_{11} & A_{12} \\ A_{12} & A_{11}\end{bmatrix}\right\}\begin{bmatrix}x_1\\x_2\end{bmatrix}=[0]$$

where the column vector is

$$[S_1]=\begin{bmatrix}x_1\\x_2\end{bmatrix}.$$

The corresponding matrix equation is

$$x_1 - x_2 = 0\,.$$

Thus, the solution vector corresponding to λ_1 is

$$[S_1]=\begin{bmatrix}x_1\\x_2\end{bmatrix}=\begin{bmatrix}1\\1\end{bmatrix}. \tag{4-32}$$

Similarly, the eigenvector corresponding to λ_2 is

$$[S_2]=\begin{bmatrix}x_3\\x_4\end{bmatrix},$$

which results in

$$x_3 + x_4 = 0\,.$$

Thus, the solution vector becomes

$$[S_2]=\begin{bmatrix}x_3\\x_4\end{bmatrix}=\begin{bmatrix}1\\-1\end{bmatrix}. \tag{4-33}$$

Hence, finally, the voltage eigenmatrix becomes

$$[S_v]=[[S_1]\quad[S_2]]=\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}. \tag{4-34}$$

The current eigenmatrix can be determined without solving eigenvalue equations by plugging (4-27), (4-28) and (4-34) into (4-12) as

$$[S_i] = \begin{bmatrix} \frac{1}{Z_1} & \frac{1}{Z_2} \\ \frac{1}{Z_1} & -\frac{1}{Z_2} \end{bmatrix} \tag{4-35}$$

where $Z_1 = \sqrt{\frac{Z_{11} + Z_{12}}{Y_{11} + Y_{12}}}$ *and* $Z_2 = \sqrt{\frac{Z_{11} - Z_{12}}{Y_{11} - Y_{12}}}$,

Inserting (4-34) and (4-35) into (4-29), the characteristic impedance is

$$[Z_c] = \frac{1}{2}\begin{bmatrix} Z_1 + Z_2 & Z_1 - Z_2 \\ Z_1 - Z_2 & Z_1 + Z_2 \end{bmatrix}. \tag{4-36}$$

Note both the propagation constant matrix and the characteristic impedance matrix have been represented by the interconnect series impedance matrix of (4-3) and the interconnect parallel admittance matrix of (4-4). Equation (4-3) and (4-4) relate directly to interconnect circuit parameters, which are discussed in section 4.6.

4.5 Characteristic Impedance Matrix and S-Parameters

Characteristic impedance matrices are important electrical parameters of multiconductor circuits. In this section, the characteristic impedance is formulated in terms of measured network parameters (s-parameters). This result is very important because microwave simulations of interconnect response can be compared and verified with microwave measurement. Thereby it is possible to investigate the physical meaning of the characteristic impedance matrix in multiconductor circuits. Finally, direct experimental transmission-line parameter extraction using mathematical analysis is discussed and shown to be intractable. A simplified parameter extraction strategy is developed in section 4.6.

Many of the physical concepts used in the derivation of single-line signal propagation can be directly extended to multiconductor lines as in Fig. 4-2. The reflection coefficient, Γ, in single line interconnect has the following form [Ram65],

$$\Gamma = \{Z + Z_0\}^{-1}\{Z + Z_0\} \tag{4-37}$$

where Z is the input impedance of the conductor looking in from the reference plane. The scattering parameter matrix for reflection and transmission in multiconductors will have a similar form. To derive the relationship between the characteristic impedance matrix and the scattering parameter matrix in a multiconductor system, generator and port voltages at port-i are defined as

$$V_{Gi} = Z_0 I_i + V_i \tag{4-38}$$

and therefore,

$$V_i = V_{Gi} - Z_0 I_i \triangleq V_i^+ + V_i^-. \tag{4-39}$$

Representing the voltage and current at port n as the incident and reflected waves,

$$\begin{cases} V_n = V_n^+ + V_n^- \\ I_n = I_n^+ - I_n^- = \frac{1}{Z_{cn}}(V_n^+ - V_n^-) \end{cases} \tag{4-40}$$

where Z_{cn} is the characteristic impedance of conductor n. Thus, for the n conductor system,

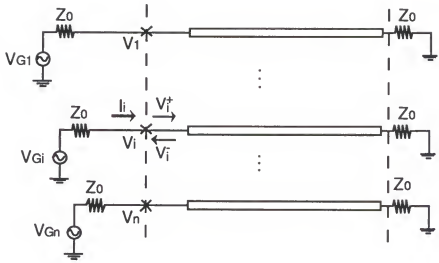


Fig. 4-2 A multiconductor system. All loads are terminated with Zo.

$$[V] = [V^+] + [V^-] = [Z][I] = ([Z_c] + [Z_o])[I] \ . \tag{4-41}$$

Combining (4-11) and (4-28), the current vector becomes

$$[I] = [Z_c]^{-1}\left([S_u][E(x)][C_1] - [S_u][E(x)]^{-1}[C_2]\right). \tag{4-42}$$

Then, from (4-10) and (4-29) the current vector can be represented in terms of voltage waves,

$$[I] = [Z_c]^{-1}([V^+] - [V^-]) \ . \tag{4-43}$$

Thus, (4-41) is rewritten

$$[V^+] + [V^-] = ([Z_c] + [Z_o])[Z_c]^{-1}([V^+] - [V^-]) \ . \tag{4-44}$$

Here, defining normalized matrix $[Z]$ as

$$[Z] \triangleq ([Z_c] + [Z_o])[Z_c]^{-1} \ , \tag{4-45}$$

(4-44) is simplified. The microwave literature refer to the matrix [Z] as impedance even though it is a normalized quantity. This dissertation will refer to [Z] as the impedance matrix, too. Then (4-44) become

$$[V^+] + [V^-] = [Z]([V^+] - [V^-]) \ . \tag{4-46}$$

Rearranging (4-46), the reflected voltage wave become

$$[V^-] = \{[Z] + [U]\}^{-1}\{[Z] - [U]\}[V^+] \tag{4-47}$$

where $[U]$ is the unit matrix and impedance matrix $[Z]$ implicitly includes the characteristic impedance matrix.

In contrast, the scattering parameter definition in multiport networks is

$$\begin{bmatrix} \frac{V_1^- \sqrt{Re(Z_{L1})}}{Z_{L1}} \\ \frac{V_2^- \sqrt{Re(Z_{L2})}}{Z_{L2}} \\ \vdots \\ \frac{V_n^- \sqrt{Re(Z_{Ln})}}{Z_{Ln}} \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots\cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots\cdots & S_{nn} \end{bmatrix} \begin{bmatrix} \frac{V_1^+ \sqrt{Re(Z_1)}}{Z_1^*} \\ \frac{V_2^+ \sqrt{Re(Z_2)}}{Z_2^*} \\ \vdots \\ \frac{V_n^+ \sqrt{Re(Z_n)}}{Z_n^*} \end{bmatrix}. \tag{4-48}$$

This is represented by the following simple matrix equation for real $Z_1 = Z_2 = \cdots = Z_n = Z_0$ and for real $Z_{L1} = Z_{L2} = Z_{Ln} = \cdots = Z_0$,

$$[V^-] = [S][V^+]. \tag{4-49}$$

The concept of scattering parameters and scattering parameter measurements are discussed in Chapter 2. Network analyzer equipment calibration is discussed in Appendix A. Combining (4-47) and (4-49),

$$[S] = \{[Z] + [U]\}^{-1}\{[Z] - [U]\}. \tag{4-50}$$

Hence, the impedance matrix is formulated in terms of s-parameters,

$$[Z] = \{[U] + [S]\}\{[U] - [S]\}^{-1}. \tag{4-51}$$

The interconnect characteristic impedance matrix has been derived in terms of measured microwave network parameters, (s-parameters). The impedance matrix is implicitly related to the characteristic impedance

matrix by (4-45). This means that the characteristic impedance in the frequency domain can be directly related to s-parameter measurements. Since (4-51) is very complicated, it is a difficult formula for direct transmission parameter extraction from s-parameters [Sch90]. Direct parameter extraction means the determination of multiconductor interconnect propagation constants and characteristic impedances from s-parameter data and (4-51). The additional difficulty in accurate calibration of multiport microwave network measurements makes direct multiconductor parameter extraction intractable. Furthermore, (4-51) is a lumped approximation model and direct coupling parameter extraction may not be practical. Thus, to extract the transmission parameters experimentally a simplified method will be introduced. This new method will be discussed in the next section.

4.6 Extraction of Coupling Parameters

The exact coupling parameter extraction for a lossy multiple transmission line system in terms of s-parameter measurements cannot be easily realized. It is conceptually very difficult to relate the measurable interconnect quantities with model parameters and it is difficult to de-embed pad parasitics in multiport networks.

However, a good approximation is possible because the frequency dependence of coupling parameters is very weak and electromagnetic interaction between lines is dominated by coupling capacitance and mutual inductance. This is so because 1) the frequency dependence of interconnect line parameters is mainly due to the skin effect (see Appendix D) and silicon substrate effects and 2) resistive and conductive coupling are

a second order loss mechanism. In addition, the self referenced parameters except self capacitance (diagonal elements of the multiconductor interconnect transmission parameter matrices) are close to those of single lines. The key result is the development of an efficient simplified model for two conductor interconnect coupling. This new model removes second order features and reduces measurement and test structure complexity.

The matrix parameters that need to be determined for modeling two-conductor interconnect signal propagation and coupling are

$$[R(\omega)] = \begin{bmatrix} R_{11}(\omega) & R_{12}(\omega) \\ R_{21}(\omega) & R_{22}(\omega) \end{bmatrix} \qquad [C(\omega)] = \begin{bmatrix} C_{11}(\omega) & -C_{12}(\omega) \\ -C_{21}(\omega) & C_{22}(\omega) \end{bmatrix}$$

$$[G(\omega)] = \begin{bmatrix} G_{11}(\omega) & -G_{12}(\omega) \\ -G_{21}(\omega) & G_{22}(\omega) \end{bmatrix} \qquad [L(\omega)] = \begin{bmatrix} L_{11}(\omega) & L_{12}(\omega) \\ L_{21}(\omega) & L_{22}(\omega) \end{bmatrix} \tag{4-52}$$

From the assumptions of equivalent self and single-line (except self capacitance) parameters, the components of the coupled line parameter matrices can be approximated as

$$R_{11}(f) \approx R_{single\text{-}line}(f) \tag{4-53}$$

$$G_{11}(f) \approx G_{single\text{-}line}(f) \tag{4-54}$$

$$L_{11}(f) \approx L_{single\text{-}line}(f) . \tag{4-55}$$

Resistive coupling and conductive coupling occur due to the finite conductivity of materials. Resistive coupling models eddy currents due to magnetic field and conductive coupling models the signal paths through

dielectric material between the lines. Generally, these loss mechanisms are insignificant. Thus,

$$R_{21}(f) = R_{12}(f) \approx 0 \tag{4-56}$$

$$G_{21}(f) = G_{12}(f) \approx 0 . \tag{4-57}$$

The capacitance and the inductance matrices play a pivotal role in electrical signal coupling. Thus, they must be accurately extracted. Once the capacitance matrix is determined, then the inductance matrix can be calculated from the capacitance matrix. Since the diagonal elements of the capacitance matrix are composed of signal-to-ground capacitances and line-to-line capacitances (coupling capacitance), they can be broken into two components. The signal to ground capacitance of a single lines which is a strong function of frequency can be extracted from s-parameter measurements. The coupling capacitance (capacitance between lines) is easily acquired from low frequency measurements (see Appendix B). Then, frequency variant self capacitance of coupled lines are determined by

$$C_{11}(f) = \frac{C_{single\text{-}line}(f) - 2C_{12} + \sqrt{(C_{single\text{-}line}(f))^2 + 4(C_{12})^2}}{2} \tag{4-58}$$

$$C_{12} = C_{low\ freq} . \tag{4-59}$$

This expression is verified in the next section.

The inductance matrix can be approximately calculated from the capacitance matrix and single line s-parameter measurements. That is, the inductance matrix is

$$[L] \approx \hat{\varepsilon}_r \mu_0 \varepsilon_0 \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix}^{-1} = \begin{bmatrix} L_{single\text{-}line}(f) & L_{12} \\ L_{21} & L_{single\text{-}line}(f) \end{bmatrix} \tag{4-60}$$

where $\hat{\varepsilon}_r$ can be determined from single line s-parameter measurements. It models average dielectric constant of the many thin film layers in an IC structure. Similarly, inductance in the single line becomes

$$L_{single\text{-}line}(f) \approx \hat{\varepsilon}_r \mu_0 \varepsilon_0 C^{-1}_{single\text{-}line}(f). \tag{4-61}$$

Therefore,

$$\hat{\varepsilon}_r = (\mu_0 \varepsilon_0)^{-1} L_{single\text{-}line}(f)\, C_{single\text{-}line}(f). \tag{4-62}$$

Thus, the coupling parameter matrix is approximated as

$$\begin{aligned} Y_{11} &= (G_{11} + G_{12}) + j\omega\,(C_{11} + C_{12}) \\ &\approx G_{single\text{-}line}(f) + j\omega\,(C_{11}(f) + C_{low\,freq\text{-}12}) \end{aligned} \tag{4-63}$$

$$\begin{aligned} Y_{12} &= -G_{12} + j\omega(-C_{12}) \\ &\approx -j\omega\, C_{low\,freq\text{-}12} \end{aligned} \tag{4-64}$$

$$\begin{aligned} Z_{11} &= R_{11} + j\omega\, L_{11} \\ &\approx R_{single\text{-}line}(f) + j\omega L_{single\text{-}line}(f) \end{aligned} \tag{4-65}$$

$$\begin{aligned} Z_{12} &= R_{12} + j\omega\, L_{12} \\ &\approx j\omega L_{12}\,. \end{aligned} \tag{4-66}$$

In IC interconnect, the expressions (4-63) through (4-66) are acceptable even for fine line-widths and narrow line-spaces.

In summary, the interconnect circuit parameter matrices are

$$[\,R(\omega)] = \begin{bmatrix} R_{11}(\omega) & R_{12}(\omega) \\ R_{21}(\omega) & R_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} R_{single\text{-}line}(\omega) & 0 \\ 0 & R_{single\text{-}line}(\omega) \end{bmatrix} \tag{4-67}$$

$$[C(\omega)] = \begin{bmatrix} C_{11}(\omega) & -C_{12}(\omega) \\ -C_{21}(\omega) & C_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} C_{11}(\omega) & -C_{low\ freq\text{-}12} \\ -C_{low\ freq\text{-}12} & C_{11}(\omega) \end{bmatrix} \tag{4-68}$$

$$[G(\omega)] = \begin{bmatrix} G_{11}(\omega) & -G_{12}(\omega) \\ -G_{21}(\omega) & G_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} G_{single\text{-}line}(\omega) & 0 \\ 0 & G_{single\text{-}line}(\omega) \end{bmatrix} \tag{4-69}$$

$$[L(\omega)] = \begin{bmatrix} L_{11}(\omega) & L_{12}(\omega) \\ L_{21}(\omega) & L_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} L_{single\text{-}line} & L_{12} \\ L_{12} & L_{single\text{-}line} \end{bmatrix}. \tag{4-70}$$

Using (4-3), (4-4), (4-18), and the parameter matrices, the interconnect circuit response can be calculated in the frequency domain. Their validity will be experimentally proven by time domain measurements in Chapter 6. There this model is used successfully to predict fast signal transients, signal propagation, and coupling noise.

4.7 Test Structure Layout for the Measurements

To characterize multiconductor interconnect coupling, test structure layouts were designed at the University of Florida and fabricated using HP-25 CMOS process of Hewlett Packard. The test patterns include single lines, coupled lines, and open pads for pad parasitic effect de-embedding. The line widths of the single line are 1, 0.8, and 0.6 μm. The coupled lines were spaced 1 and 0.8 μm apart. Coupled lines are also 1 and 0.8 μm. The length of all test structures are 500 μm. Pads are 100 μm by 100 μm. The detailed layout of the test structure is shown on Fig. 4-4. The test patterns are shown on Fig. 4-5.

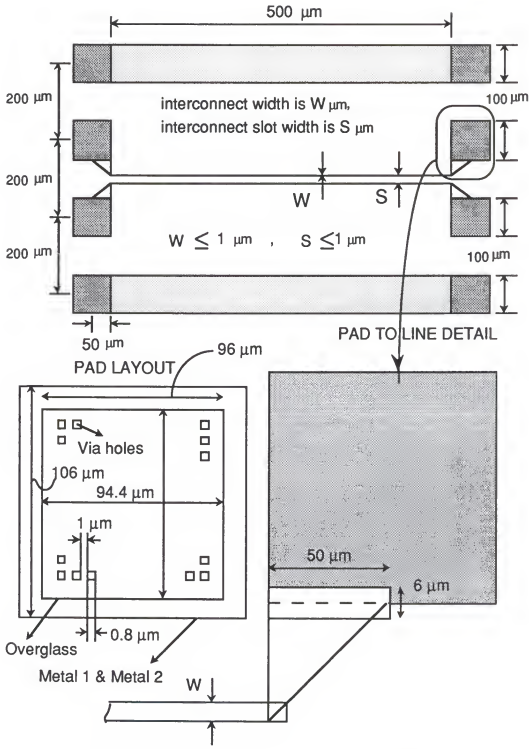


Fig. 4-3 Coupled line test structure and pad.

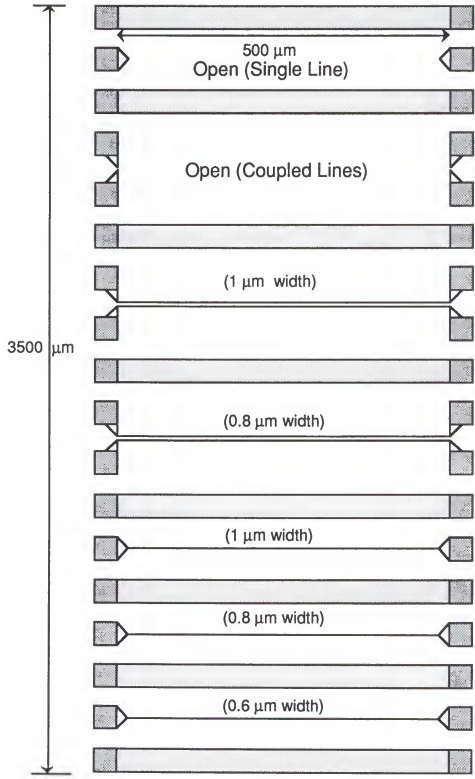


Fig. 4-4. IC test structure layout.

S-parameter measurements were performed for the single and multiconductor structures. Measurements of the single conductor lines were good but exhibited noise above 10 GHz. The multiconductor structures exhibited a lot of noise at all frequencies. This was due to 1) the short length of the lines, 2) the non-symmetry of the GSS (Ground-Signal-Ground) probes for multiconductor structures, 3) the domination of parasitic effects (pad parasitics) over DUT response. Thus, the s-parameter test methodology for multiconductor lines needs further improvements and refinement for more accuracy.

An alternative set of low frequency capacitance measurements were performed. Low frequency capacitance measurements of the HP structures are shown on the Table 4-1 which includes the single line self capacitance, C_{single}, coupling capacitance, $C_{12\text{-}low}$, self-coupled line capacitance, $C_{11\text{-}low}$, self capacitance calculated from (4-58), and dc resistance, $R_{single\text{-}dc}$. From these low frequency self and coupling capacitances measurements, the important expression (4-58) for multiconductor circuits is experimentally verified. The calculated values of C_{11} using (4-58) (in table column 5) agree with the measured values of $C_{11\text{-}low}$ (in table column 3) within about 5 %. The calculation is done using C_{single} and $C_{12\text{-}low}$ in Table 4-1 to yield the calculated C_{11} values. As is expected, the single line self capacitance, C_{single}, is larger than coupled line self capacitance, $C_{11\text{-}low}$. Also, coupling capacitance, $C_{12\text{-}low}$ is comparable in magnitude to the self capacitance, $C_{11\text{-}low}$. This implicitly indicates that the crosstalk noise will be a serious problem for the high performance VLSI circuit designs.

Table 4-1 Low frequency capacitance and resistance parameters which are averages of results of repeated measurements. Distance between the lines is the same as the line width.

(pF/unit length*, ohm/unit length)

Width	Measured C_{single}	Measured $C_{11\text{-}low}$	Measured $C_{12\text{-}low}$	Calculated $C_{11\text{-}low}$ from (4-58)	Measured $R_{single\text{-}dc}$
1 μm	0.046	0.0337	0.0267	0.031	36.5
0.8 μm	0.042	0.0283	0.032	0.027	42.5
0.6 μm	0.036	/	/	/	53.7

* unit length is 500 μm

4.8 Summary and Discussion

Signal coupling becomes more and more significant as the distance between lines is reduced. Using too conservative VLSI design rules to mitigate electromagnetic coupling requires excessive die area and reduces design flexibility. Exact characterizations are extremely useful for next-generation VLSI circuit designs with design rules on the order of 0.5 μm.

The multiconductor signal behavior is mathematically modeled by using a matrix form of the Telegrapher's equations with multiconductor line parameter matrices. The solution vectors of Telegrapher's equations are presented in terms of propagation constants and characteristic impedances. It was shown that these solution vectors are direct functions of interconnect line parameter matrices. Thus, the exact determination of line parameter matrices is the key to predicting electrical signal variation on lossy fine line VLSI interconnects. In this chapter, the multiconductor transmission line equations with terminal networks have been solved. The line parameter matrices which relate the mathematical model to the physical properties of interconnect systems are presented.

A primary contribution of this chapter is a development of the approximate parameter extraction method. The method combines single line scattering parameter measurements and low frequency capacitance measurements. A new self-capacitance expression for coupled lines is derived. The validity of the new expression is experimentally proven using submicron HP interconnect test structures. Moreover, from test structure coupling parameter measurement, the self capacitance and coupling capacitance have comparable magnitudes in submicron structures. However, today's VLSI circuits have self capacitance that dominates the

coupling capacitance. Thus, a key for the next generation of VLSI circuit designs is the exact characterization of signal coupling. Accordingly, the simplified model is extremely valuable because it requires only single line s-parameter measurements and low frequency capacitance measurements. It will be very useful in developing design rules for the next generation of VLSI circuits.

CHAPTER 5
HIGH SPEED VLSI INTERCONNECT MODELING BASED ON S-PARAMETER MEASUREMENTS

5.1 Introduction

The mathematical analysis of multiconductor interconnect systems and experimental techniques to provide interconnect circuit parameters were presented in Chapter 4. The key experimental parameters are the interconnect parameter matrices, $[R]$, $[L]$, $[C]$, and $[G]$. However, experimental techniques cannot provide predictive analysis for future technologies. Also an interconnect experimental data base is limited by the accessibility of IC test structures. IC test structures are expensive and require many months for fabrication.

An important alternative is to develop physical models for the $[R]$, $[L]$, $[C]$, and $[G]$ interconnect circuit parameter matrices. This provides predictive modeling capability and extends modeling to regions not covered by experimental test structures. However, a comprehensive set of interconnect circuit parameter models that incorporate high frequency effects has not been done prior to this work.

As shown in Chapter 3, interconnect s-parameter measurements demonstrate frequency dependent capacitance, conductance, and resistance at high frequencies [Eis92]. Additional resistive effects due to the fine line lithography and inductive effects due to high frequencies can be important. As discussed already, in Chapter 1 and Chapter 3, errors

introduced by simple RC ladder models may introduce modeling inaccuracies in the highest performance VLSI circuits.

New interconnect circuit parameter models based on s-parameter measurements are reported in this chapter. Existing IC interconnect models [Sak83, Yua82b, Sch69, Has71] assume one of or all of the followings: constant parameter values with frequency, no fringing effects, and no silicon substrate conductance effects. This work extends existing interconnect models to include the above effects and introduces a model for first-level VLSI interconnect that is valid through GHz frequencies.

Interconnect parameters calculated with these models have been compared with values extracted from s-parameter measurements. They show excellent agreement. Furthermore, PISCES-IIB simulation, low frequency measurements, and dc measurements of the IC interconnect test structures have been performed. They also verify the validity of the models.

The chapter is organized as follows. A characterization section reviews IC test structure designs and s-parameter measurements. Then, low frequency first order modeling of interconnect is presented, followed by more general frequency variant modeling of IC interconnect line. Finally, the influence of inductance in high frequency propagation is reported.

5.2 S-Parameter Characterization of Interconnects

Signal propagation in single-line interconnect is modeled by the Telegrapher's equation. The frequency variant model parameters of the Telegrapher's transmission-line equation for IC interconnect have been extracted directly from s-parameter measurement data [Eis92]. The

standard form of the voltage and current traveling wave solution to the Telegrapher's equation is

$$\begin{cases} V = V^+e^{-\gamma x} + V^-e^{+\gamma x} \\ I = \frac{1}{Z}\left[V^+e^{-\gamma x} - V^-e^{+\gamma x}\right] \end{cases}, \qquad (5\text{-}1)$$

$$where \quad \gamma = \sqrt{Z_s Y_p} = \sqrt{(R + j\omega L)(G + j\omega C)}\,.$$

In order to solve the above equations, the propagation constant, γ, and characteristic impedance, Z , of the interconnect must be known. These two important parameters are composed of a series impedance, Z_s (= R + $j\omega L$), and a parallel admittance, Y_p (= $G + j\omega$C). The line parameters (Z, γ, R, L, C, and G) are extracted from s-parameter measurements. Reviewing the results of Chapter 3,

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \qquad (5\text{-}2)$$

$$where \quad K = \left\{ \frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}}$$

$$Z^2 = Z_0^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} = \frac{(R + j\omega L)}{(G + j\omega C)}\,. \qquad (5\text{-}3)$$

Then,

$$\begin{aligned} R &= Re\,\{\gamma Z\} \\ L &= Im\,\{\gamma Z\}/\omega \\ G &= Re\,\{\gamma/Z\} \\ C &= Im\,\{\gamma/Z\}/\omega\,. \end{aligned} \qquad (5\text{-}4)$$

In general, pad-parasitic response must be subtracted from test-structure response in high-frequency characterizations. This is discussed in the literature [Eis92, Wij87] and in Chapter 3.

5.3 Static Interconnect Circuit Parameter Modeling

5.3.1 Typical RC-Based Interconnect Models

Typically an interconnect has been modeled using an RC ladder circuit [Bak85]. The model parameters have been calculated by expressions based on layout geometrical configurations, thin film sheet resistances, thin film capacitances, and by expressions in the literature. The resistance of a line of length, L, thickness, t, and width, w, is generally given as,

$$R = \rho \frac{L}{tW} = R_s \frac{L}{W} \tag{5-5}$$

where ρ is the resistivity of interconnect material and R_s is the sheet resistance based on dc measurements. In this simple model, the resistance calculation is straightforward. In reality, at high frequency, the resistance of interconnect become a function of frequency due to the skin effect and causes large conductive loss. Furthermore, manufacturing variations in interconnect thickness and the surface roughness of the thin film conductor affect the interconnect resistance.

There are many models and expressions for calculating interconnect capacitance based on the layout and cross-section of geometrical configurations. An empirical capacitance equation for the metal-oxide-silicon structure (see Fig. 5-1) is frequently used for interconnect and circuit simulation [Sak83]. The capacitance of a section of

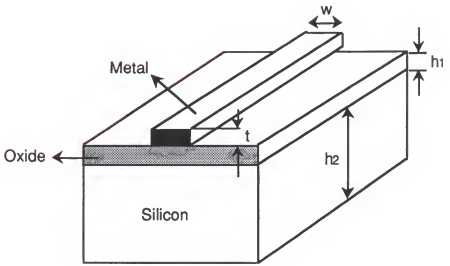


Fig. 5-1 Metal-oxide-silicon interconnect structure.

interconnect of length, l, on the stacked layers of the oxide and bulk silicon is given by [Sak83]

$$C = \varepsilon_{ox}\left\{1.15\left(\frac{w}{h_1}\right) + 1.40\left(\frac{t}{h_1}\right)^{0.222}\left(2 + 2\frac{w}{l}\right) + 4.12\left(\frac{t}{h_1}\right)^{0.728}\left(\frac{h_1}{l}\right)\right\}. \qquad (5\text{-}6)$$

Variables are defined in Fig. 5-1. Using this empirical expression, the capacitances of 2 μm, 4 μm, and 10 μm test structures can be calculated. Table 5-1 shows results of low frequency C-V meter measurements at 1 kHz (see Appendix B), s-parameter measurements, modeling using of (5-6), and PISCES-IIB simulation of capacitance. These results agree for frequencies between 1 kHz and 45 MHz for all interconnect widths. However, (5-6) does not model silicon substrate high frequency properties. Direct s-parameter measurement is required to find high frequency capacitance. The silicon substrate has additional propagation modes controlled by the doping concentration and frequency [Has71].

The simple RC ladder model of first level metal IC interconnect does not model frequency variant properties of the interconnect signal propagation, dielectric loss, or inductance. These result in significant deviation for capacitance above 1 GHz and resistance at several GHz. Frequency variant interconnect properties are important at microwave frequencies and clock frequencies greater than 100 MHz as discussed in Chapter 3. Thus, simple RC ladder models are not suitable for very high frequency circuit design and simulation.

Table. 5-1 Capacitance comparison from various simulation and measurement methods (unit is pF/cm).

Method of Capacitance Determination	Interconnect width		
	2 μm	4 μm	10 μm
Modeling using expression (5-6)	1.23	1.62	2.81
C-V Measurement (at 1 kHz)	1.08	1.36	2.41
S-Par. Measure (at 45 MHz)	0.98	1.34	2.29
S-Par. Measure (at 20 GHz)	0.59	0.65	0.76
PISCES-II (below 1 MHz)	0.95	1.33	2.41

5.3.2 Invariant Parameter RLCG Interconnect Models

A simple extension of the RC model is to a frequency invariant RLCG model. Early work in interconnect modeling developed analytical expressions for IC interconnect parameter extraction for the frequency invariant RLCG model. This work will be discussed below with the most accurate results presented.

Early work shows that the metal-oxide-silicon interconnect structure has three fundamental propagation modes, quasi-TEM mode, skin-effect mode, and slow-wave mode [Has71]. An invariant parameter model (RLCG) which is more complicated than the simple RC model is required for higher frequencies. The basic model structure and its equivalent circuit are shown in Fig. 5-1 and Fig. 5-2, respectively. Telegrapher's equation-based RLCG interconnect line parameter models of Fig. 5-3 have been derived by considering silicon substrate properties as well as inductance and dielectric loss [Sch69, Has71]. These models have proven acceptable for wide interconnect and moderate frequency. The line parameters of Fig. 5-2 are given by [Has71]

$$L = \mu_0 F(h_2 + h_1 , w) \tag{5-7}$$

$$R = \frac{1}{\sigma_{metal} wt} \tag{5-8}$$

$$C_1 = \frac{\varepsilon_0 \varepsilon_{eff}(\varepsilon_{sio_2}, h_1)}{F(h_1, w)} \tag{5-9}$$

$$C_2 = \frac{\varepsilon_0 \varepsilon_{eff}(\varepsilon_{si}, h_2)}{F(h_2, w)} \tag{5-10}$$

$$G_s = \frac{\sigma_{si}[\, 1 + (1 + 10 h_2 / w)^{-1/2} \,]}{2F(h_2, w)} \tag{5-11}$$

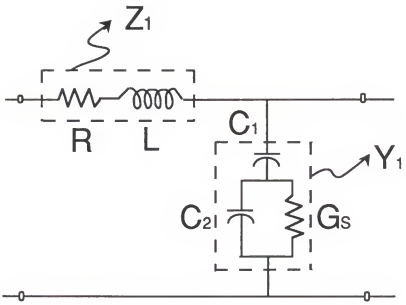


Fig. 5-2 IC interconnect cross section configuration-based interconnect circuit model.

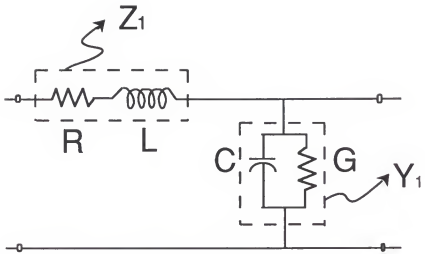


Fig. 5-3 Telegrapher's equation-based model representation of single conductor interconnect.

$$F(h,w) = \begin{cases} \frac{1}{2\pi} ln(8h/w + w/4h) & ; h/w \geq 1 \\ \frac{1}{w/h + 2.42 - 0.44h/w + (1- h/w)^6} & ; h/w \leq 1 \end{cases} \quad (5\text{-}12)$$

$$\varepsilon_{eff}(\varepsilon,h) = \frac{\varepsilon + 1}{2} + \frac{\varepsilon - 1}{2(1 + 10h/w)^{1/2}}. \quad (5\text{-}13)$$

Here, $h = h_1 + h_2$ and the rest of the variables are defined in Fig. 5-1. The above model of capacitance for wide line interconnect agrees with the experimental values as well as PISCES-IIB simulation of the capacitance [Eo90].

However, even at the low frequencies, this constant parameter RLCG model disagrees in substrate capacitance, conductor resistance, and inductance in fine line interconnect. The parameter extraction is done poorly for fine line interconnect. Furthermore, since these interconnect parameters vary with frequency, more accurate models are required for high frequency signals on fine line interconnect. A new frequency variant model is developed for fine line IC interconnect in the next section.

5.4 Frequency Variant Interconnect Modeling

5.4.1 Frequency Variant Resistance Modeling

As frequency increases, conductor resistance becomes controlled by the skin effect. At high frequency an infinitely thick conductor supports an exponentially decaying current density from the surface to the center. The skin depth represents an equivalent depth in which an uniform current density would flow. At high frequencies the conducting electrons of a metal are confined close to the surface of a conductor within a skin depth.

Frequency dependent conductor loss has been derived by using the incremental inductance rule [Whe42], but this analysis assumes conductor thickness should be much less than a skin depth i.e., $\delta \leq 0.1t$ [Deu90, Puc68]. However, for modern ICs, the conductor thickness is roughly equal to skin depth, δ, (A skin depth is defined in Appendix D). Therefore, the incremental inductance rule introduces error.

If the conductor thickness is comparable to the skin depth, an effective one dimensional skin depth can be computed (see Appendix D),

$$\delta_x = \delta\left\{1 - exp\left(-\frac{t}{\delta}\right)\right\}, \qquad (5\text{-}14)$$

$$where \quad \delta = \frac{1}{\sqrt{\pi f \mu / \rho}}.$$

For microstrip, an empirically modeled sidewall current has been developed (see Appendix D),

$$\delta_y = \delta_x \frac{t}{w}. \qquad (5\text{-}15)$$

Therefore, the total effective skin depth, δ^*, becomes

$$\delta^* = \delta_x + \delta_y = \delta_x\left(1 + \frac{t}{w}\right). \qquad (5\text{-}16)$$

Since

$$R_s = \frac{\rho}{\delta^*},$$

$$R = R_s\left(\frac{l}{w}\right) = \frac{\rho}{\delta^*}\left(\frac{l}{w}\right)$$

$$= \frac{\rho}{\delta\left\{1 - exp\left(-\frac{t}{\delta}\right)\right\}\left(1 + \frac{t}{w}\right)}\left(\frac{l}{w}\right). \qquad (5\text{-}17)$$

Thus, the resistance model is,

$$R = \begin{cases} R_{dc} & ; if \quad R(f) < R_{dc} \\ R(f) = \dfrac{\rho}{\delta\left(1 - exp(-\dfrac{t}{\delta})\right)\left(1 + \dfrac{t}{w}\right)}\left(\dfrac{l}{w}\right) & ; if \quad R(f) > R_{dc} \end{cases}$$

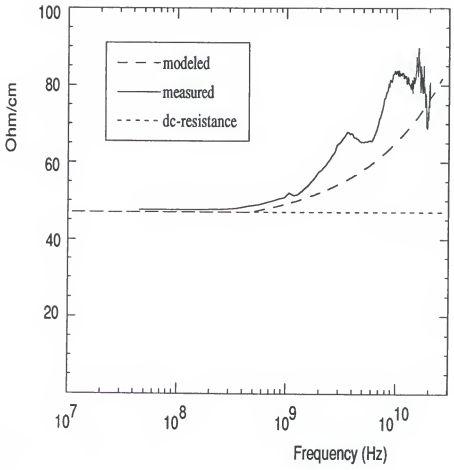
$$where \quad \delta = \frac{1}{\sqrt{\pi f \mu \rho}}. \qquad (5\text{-}18)$$

In the above equation, the resistivity of the conductor can be characterized by dc measurements.

The resistance values calculated according to the above modeling and those of the s-parameter measurements are shown on the Fig. 5-4. This resistance model is superior to the thin film resistance described by the RC model equation (5-5) as seen in Fig. 5-4. The error for the thin film resistance (5-5) increases drastically just after the frequency that skin effect occurs. However, the excellent agreement of (5-18) with experimental data verifies that the aforementioned resistance model is suitable for the modern high frequency and narrow interconnect line.

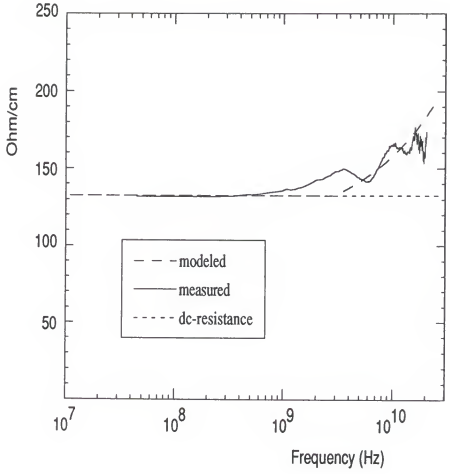
5.4.2 Frequency Dependence of Dielectric Constant

For the sake of completeness, the effects of the frequency variation of the dielectric constant should be discussed. These effects occur above about 10 ~ 20 GHz and are due to a change in the propagation mode on microstrip [Goo89, Pra83, Yua91]. Previous static models for capacitance and dielectric loss must be modified for the highest performance VLSI



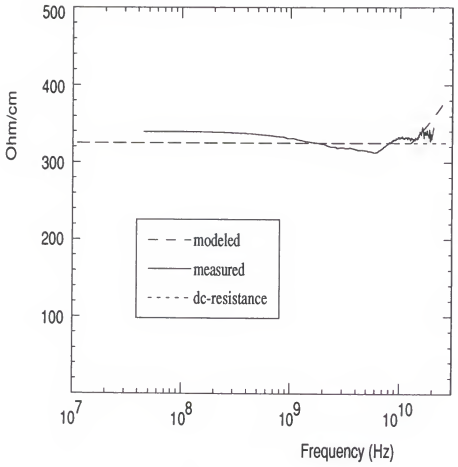
(a) 10 μm width.

Fig. 5-4 Resistance variation of s-parameter measurements and model values.



(b) 4 μm width.

Fig. 5-4--continued.



(c) 2 μm width.

Fig. 5-4--continued.

circuits or microwave circuits of the future, although this modeling is not required for current silicon VLSI circuits.

The frequency dependent dielectric constant is given by [Pra83],

$$\varepsilon_r(f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}}{(1 + f^2/f_t^2)} \tag{5-19}$$

where f_t is the cut-off frequency of the lowest order TE mode of the microstrip, given by

$$f_t = \frac{c^2 Z_0 \varepsilon_0 \varepsilon_r}{2h\sqrt{\varepsilon_{eff}\,\varepsilon_r}} \tag{5-20}$$

where c is velocity of light and Z_0 is the characteristic impedance given by [Whe77],

$$Z_0 = \frac{120\pi F(h,w)}{\sqrt{\varepsilon_{eff}}}. \tag{5-21}$$

5.4.3 Frequency Variant Capacitance and Dielectric Loss

Determining interconnect circuit parameter models for the Telegrapher's equation is the goal of this chapter. Thus, the lossy silicon substrate interconnect model of Fig. 5-2 must be transformed to Telegrapher's equation circuit model of Fig. 5-3. The lossy interconnect circuit model of Fig. 5-2 is derived directly from the interconnect cross section of Fig. 5-1. The equivalent Telegrapher's equation model in terms of the lossy silicon IC cross section in performed below. Note that for the multilayer of oxide and nitride the capacitance C_1 of Fig. 5-2 is

$$\frac{1}{C_1} = \frac{1}{C_{ox1}} + \frac{1}{C_{nitride}} + \frac{1}{C_{ox2}}. \tag{5-22}$$

The equivalent admittance for the solution to the Telegrapher's equation in terms of the silicon substrate cross section is

$$Y_1 = \frac{\omega^2 C_1^2 G_s}{G_s^2 + \omega^2 (C_1 + C_2)^2} + j\omega \frac{\omega^2 C_1 C_2 (C_1 + C_2) + C_1 G_s^2}{G_s^2 + \omega^2 (C_1 + C_2)^2}$$

$$= G + j\omega C . \tag{5-23}$$

Therefore, the Telegrapher's equation G and C are

$$G = \frac{\omega^2 C_1^2 G_s}{G_s^2 + \omega^2 (C_1 + C_2)^2} \tag{5-24}$$

$$C = \frac{\omega^2 C_1 C_2 (C_1 + C_2) + C_1 G_s^2}{G_s^2 + \omega^2 (C_1 + C_2)^2} . \tag{5-25}$$

Equations (5-24) and (5-25) prove that there will be a frequency variation in the circuit parameters used to describe signal propagation on the silicon substrate. The low frequency and high frequency asymptotic values of (5-24) and (5-25), are

$$\begin{cases} \lim_{\omega \to 0} G = 0 \\ \lim_{\omega \to 0} C = C_1 \end{cases} \tag{5-26}$$

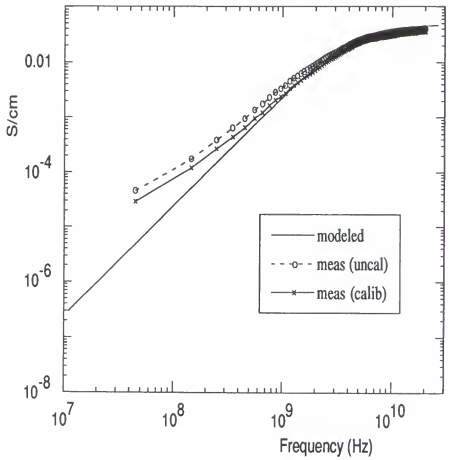
$$\begin{cases} \lim_{\omega \to \infty} G = \dfrac{C_1^2 G_s}{(C_1 + C_2)^2} \\ \lim_{\omega \to \infty} C = \dfrac{C_1 C_2}{C_1 + C_2} \end{cases} . \tag{5-27}$$

Expressions (5-26) and (5-27) show that dielectric loss due to silicon substrate conductance cannot be neglected at high frequency even if it is negligible at low frequency. Also, there exist transition regions in which

the signal propagation mode changes from the slow wave mode (5-26) to the quasi-TEM mode (5-27). Circuit simulation with constant parameters using SPICE is feasible for limited bandwidths at these asymptotic values. By using these equations the simulation error in existing models can be estimated and a simulation cost versus model complexity tradeoff can be performed. For a given technology it is possible to estimate at what frequencies silicon substrate loss and capacitance become important. The dielectric loss of the silicon substrate is frequency dependent. The values calculated by (5-24) agree well with s-parameter measurements for narrow strip to wide strips. The dielectric loss calculated by using (5-24) and the measured values are plotted in Fig. 5-5. From Fig. 5-5, the de-embedded values verify that pad parasitics must be subtracted and dielectric loss is not negligible at high frequency. Note, there is no dielectric loss included in the standard RC model of silicon interconnect.

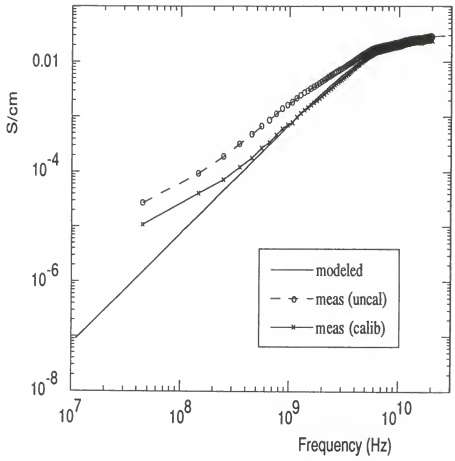
5.4.4 Fringing Capacitance

The typical RC model does not take into account conductor thickness effects. A conductor that has a height similar to its width will have additional fringing capacitance. This is becoming increasingly important for fine line IC interconnect because conductor area must be maintained large to avoid electromigration problems. In particular, the static line parameter expressions given by (5-7) to (5-13) do not take the fringing effects of a thick conductor into account. Even at low frequency, the fringing effects of the narrow and thick conductor strips is not negligible. The low frequency fringing effect is modeled by using a cylindrical approximation [Yua82],



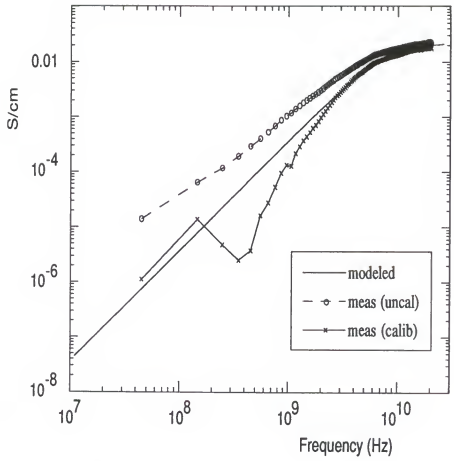
(a) 10 μm width.

Fig. 5-5 Conductance variation of s-parameter measurements and model value.



(b) 4 μm width.

Fig. 5-5--continued



(c) 2 μm width.

Fig. 5-5-continued

$$C_f = \varepsilon \frac{2\pi}{ln\left[1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right]} \tag{5-28}$$

where ε is the double layered dielectric constant. In previous work, ε is defined as the average dielectric constant of a double layer dielectric using the algebraic average [Yua82],

$$\varepsilon = \frac{1}{2}(\varepsilon_1 + \varepsilon_2)\varepsilon_0 . \tag{5-29}$$

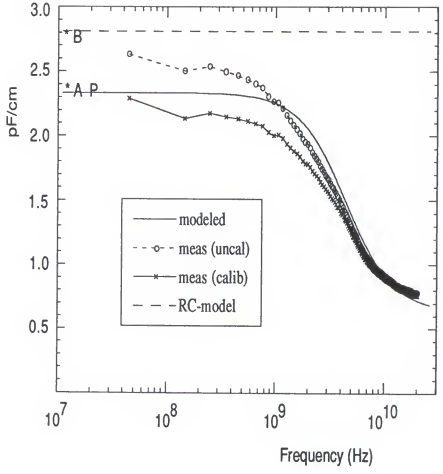
An empirical model that better fits the data describes the dielectric constant of the two layers as a series connection of two capacitances, then the average dielectric constant becomes

$$\varepsilon = \frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}\varepsilon_0 . \tag{5-30}$$

Letting $\varepsilon_1 = \varepsilon_{sio_2}$ and $\varepsilon_2 = \varepsilon_{si}$, the relative dielectric constant of the double layer is $\varepsilon_r \approx 2.93$ i.e., $\varepsilon \approx 2.93 * \varepsilon_0 = 0.26\, pF/cm$ using (5-30). The fringing capacitance of the interconnect of the interconnect test structures is $C_f \approx 0.225\, pF/cm$. Since this fringing capacitance is in parallel with the oxide capacitance, the total capacitance becomes

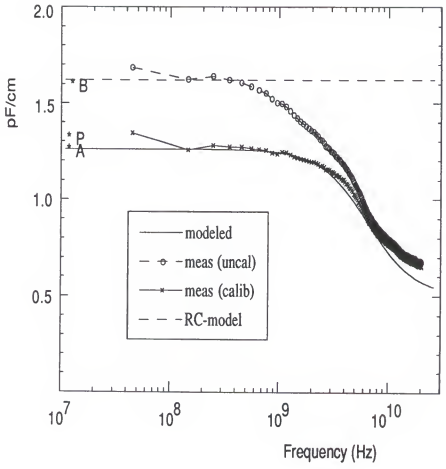
$$C_T = C + C_f . \tag{5-31}$$

This capacitance model of C_T shows excellent agreement with experimental values in narrow strips. The capacitance variation with frequency is shown on Fig. 5-6. The values calculated with (5-31) have an excellent agreement with s-parameter measurement from the 2 μm narrow strips to the 10 μm wide strips.



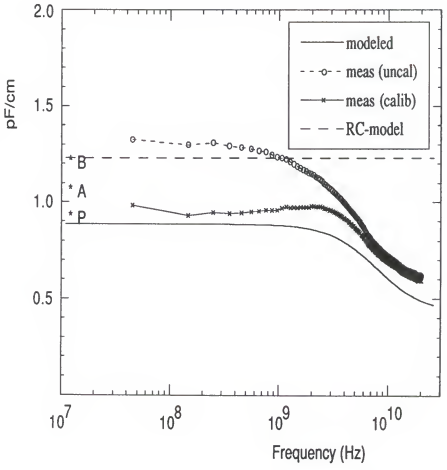
(a) 10 μm width.

Fig. 5-6 Capacitance variation, where points, "A", "B" and "P" represent low frequency measurement, empirical expression value and PISCES-II simulation, respectively.



(b) 4 μm width.

Fig. 5-6--continued



(b) 2 μm width.

Fig. 5-6--continued

This is in contrast to the typical RC capacitance model of (5-6). The maximum error in C_T compared to the measured C is at most within 10 % while error in C from the RC model (5-6) is about 30 % at low frequency and 50 % at high frequencies. To compare these values with low frequencies capacitance measurement values (at 1 kHz), equation (5-6), and PISCES-IIB simulation, points are marked as "A", "B", and "P" on Fig. 5-6, respectively. The low frequency measurements and PISCES-IIB simulations are very close to (5-31) and s-parameter measurements at 45 MHz, whereas (5-6) is a little bit larger than experimental values. Note, the value from (5-6) deviates from measurement values as frequency increases but (5-31) follows measurement values across the frequency range. Note also that Fig. 5-6 verifies that de-embedding for the pad parasitics is necessary.

In summary, the typical capacitance value (5-6) shows large discrepancies over all frequency ranges and the low frequency measurements and PISCES-IIB simulation are adequate for low frequencies, but only expression (5-31) gives excellent values for capacitance from dc to 20 GHz.

5.5 Inductance at High Frequency

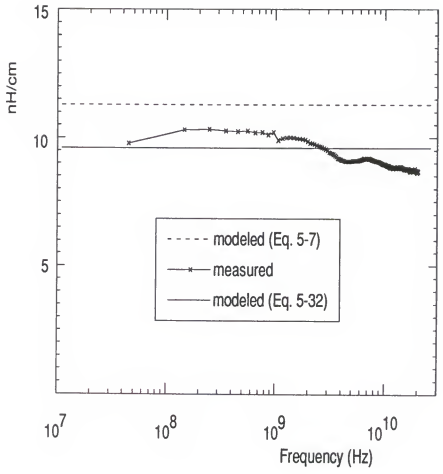
The typical RC interconnect model completely neglects inductance and silicon substrate effects. This section will show that inductance becomes important in signal propagation on IC interconnect as the frequency increases. This fact is ignored in most of the literature. Test structure measurements show that inductance is not a strong function of frequency. Moreover, although the inductance value is a function of the

interconnect cross section, it is a weak function that is proportional to the logarithm of dimensions of the conductor. Since the inductance is proportional to the total magnetic flux passing through the dielectric that is perpendicular to the signal propagation direction, it shows little variation with similar vertical structures. This is so because the permeability of common silicon IC process dielectric is unity. Inductance variation with line width is shown in Fig. 5-7.

Fig. 5-7 illustrate that the values calculated by using (5-7) and (5-12) are larger than s-parameter experimental values. Expression (5-7) yields more accurate values for a wide interconnect than for a narrow interconnect when compared with experimental values. However, the expression (5-7) overestimates the inductance value by around 20 % in Fig. 5-7. Unfortunately, expression (5-7) was derived using conformal mapping theory under the assumption that conductor thickness is zero (t = 0) [Sch69]. A rigorous solution for inductance with finite thickness can be obtained through a complicated elliptic integral. Therefore, instead of using (5-7), an expression which does not assume zero conductor thickness but square cross section is used [Whe77],

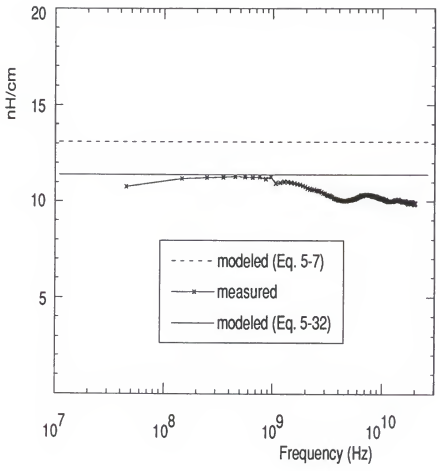
$$L = \mu_0 \frac{1}{2\pi} ln\left[\left(\frac{h}{0.59w} + 1.1\right) - 0.5 + \sqrt{\left(\frac{h}{0.59w} + 1.1\right)^2 - 1.05}\right]. \quad (5\text{-}32)$$

The inductance model values of (5-32) were plotted with s-parameter measurements values from 2 μm to 10 μm on Fig. 5-7. The model values are very close to the measurement values except for error-prone measurement data at low frequencies for 2 μm interconnect. The low frequency inductance data are error-prone since the inductive reactance

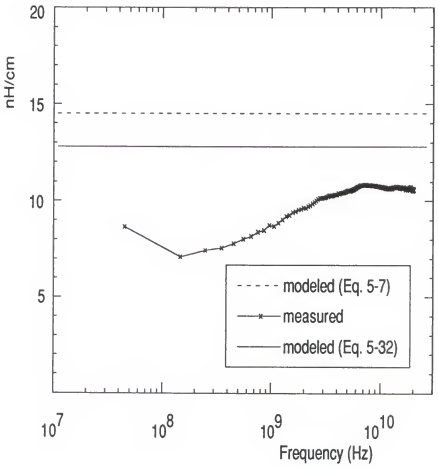


(a) 10 μm width.

Fig. 5-7 Inductance variation of s-parameter measurements and model values.



(b) 4 μm width.
Fig. 5-7-continued



(c) 2 μm width.

Fig. 5-7-continued

goes to zero as frequency decreases. Inductance become extremely important for signals on the order of 1 GHz because inductive reactance is comparable to the conductor resistance above 1 GHz.

5.6 Summary and Discussion

Typical analytic expressions for determining RC interconnect line parameters are presented. Then, the new interconnect parameter models are developed which are based on experimental values for high speed VLSI circuit designs. The new interconnect models take the silicon substrate properties, pad parasitics, fringing effects, and frequency variant properties of the circuit parameters into account. The values calculated from these models are compared with s-parameter-measurement-based extraction values as well as dc measurements, low frequency measurements, and PISCES-IIB simulation. It was shown that their agreements are excellent.

Simple RC model of interconnect signal propagation are not suitable for the highest speed VLSI circuit design. At high frequencies, dielectric loss becomes significant. There is a transition region of capacitance as frequency increases. Moreover, conductor skin effect is significant over microwave frequencies. Although inductance can be neglected at low frequencies, the inductive reactance in microwave frequencies has to be taken into account.

In microwave frequencies, not only the inductance and dielectric loss but also the frequency variant properties of the interconnect circuit parameters become important. Furthermore, through this work, more

accurate simulation using existing circuit simulation tools can be performed.

CHAPTER 6
PICO-SECOND SIGNAL TRANSIENT, PROPAGATION, AND CROSSTALK ON LOSSY FREQUENCY VARIANT VLSI INTERCONNECTS

6.1 Introduction

The problem this chapter addresses is the accurate simulation and verification of high speed coupled-signal transients on VLSI ICs. The conventional RC model is shown to be inadequate for simulation of these high speed signal transients. The frequency variant RLCG model is shown to give more accurate responses than other models in coupled interconnect simulation. The accuracy of the RLCG model is verified with on-chip picosecond time domain measurements. In order to perform high-speed interconnect circuit simulations many new results are developed. Also, the previous results in Chapter 3 through Chapter 5 are extensively used to develop the high-speed interconnect circuit simulation algorithm.

In this work, a generalized interconnect circuit model in which all the line parameters are not constant but frequency variant has been developed. The line parameter models were developed on the basis of the high frequency s-parameter measurements reported in Chapter 3 [Eo92.a]. In this previous work, the validity of the model parameters was verified with existing measurements techniques.

A new expression for the interconnect system transfer function has been derived under arbitrary load conditions, i.e., without any restrictions in circuit load impedance. Under these generalized conditions, high speed

signal variations on coupled interconnects have been simulated with differing interconnect models, line spaces, and load conditions. The newly developed interconnect simulation methodology has been verified with time domain measurements using an HP54121T high speed sampling oscilloscope.

In summary, the new research developments are: 1) an exact mathematical analysis of coupled lines, 2) a new time-domain interconnect simulation algorithm, 3) a comparison between existing interconnect models and the frequency variant RLCG model, 4) a frequency variant pad parasitic model, 5) verification of the simulation results using high-speed time domain measurements.

This work permits the accurate prediction of coupled interconnect circuit responses. With these models, signal integrity problems of high performance VLSI circuits can be solved in the design stage.

As the integration level increases, the chip area occupied by interconnects as well as the average length of the interconnect becomes greater. Furthermore, high speed operation in such high density circuits can cause unanticipated signal problems. Thus, in order to design the high density and high speed VLSI circuits, accurate knowledge of the electrical characteristics of the interconnect becomes essential so that signal delay, transient, and crosstalk problems can be avoided [Hat87, Win91, Sch89, Deu90, Goo89, Lia90].

The conventional RC interconnect circuit model is based on inaccurate assumptions. The model accounts only for capacitive coupling, assumes interconnect line parameters constant with frequency, neglects dielectric loss, and restricts circuit loading conditions. Many attempts to predict the exact interconnect responses have been made [You90, Hwa91,

Lio90, Ghi89, Win91]. However, interconnect signal variations are not accurate for high speed circuits because assumptions were made that are the same as those of the RC models.

The chapter is organized as follows. The mathematical formulations of coupled interconnects are established and the generalized transfer functions are derived and represented in terms of the interconnect line parameters. Then a line parameter extraction methodology and interconnect model are described, followed by interconnect circuit simulations in the time domain. Finally, the interconnect circuit simulations are verified with high speed sampling oscilloscope time-domain measurements.

6.2 Mathematical Formulation of Coupled Interconnects

To perform transient simulation of coupled interconnect circuits, it is necessary to construct the correct circuit transfer function. This section develops a new circuit transfer function for multiconductor coupled interconnects with frequency variant parameters. There are no restrictions on the load conditions. This is a new result and is an improvement on the transfer function presented in Chapter 4.

Electrical properties of multiconductor transmission lines can be represented by the following matrix form of the Telegrapher's equations as condensed and reviewed from Chapter 4,

$$\frac{d[V(x)]}{dx} = [Z_s][I(x)] \tag{6-1}$$

$$\frac{d[I(x)]}{dx} = [Y_p][V(x)] \tag{6-2}$$

where $[V(x)]$ and $[I(x)]$ are line voltages and currents and $[Z_s]$ and $[Y_p]$ are composed of

$$[Z_s] = [R] + j\omega[L] = \begin{bmatrix} Z_{11} & \cdots\cdots & Z_{1n} \\ \vdots & \ddots & \vdots \\ Z_{n1} & \cdots\cdots & Z_{nn} \end{bmatrix} \tag{6-3}$$

$$[Y_p] = [G] + j\omega[C] = \begin{bmatrix} Y_{11} & \cdots\cdots & Y_{1n} \\ \vdots & \ddots & \vdots \\ Y_{n1} & \cdots\cdots & Y_{nn} \end{bmatrix} \tag{6-4}$$

where

$$C_{ii} = \sum_{j=1}^{n} c_{ij} \qquad \text{and} \qquad C_{ij} = -c_{ij} \ , \tag{6-5}$$

similarly

$$G_{ii} = \sum_{j=1}^{n} g_{ij} \qquad \text{and} \qquad G_{ij} = -g_{ij} \ . \tag{6-6}$$

The propagation constant and characteristic impedance are derived by solving the eigenvalue equations. The voltage eigenmatrix, $[S_v]$, and current eigenmatrix, $[S_i]$, are the solutions of the eigenvalue equations as shown in Chapter 4,

$$\left(\gamma^2 [U] - [Z_S][Y_P] \right)[S_v] = 0 \tag{6-7}$$

$$[S_i] = [Z_S]^{-1}[S_v][\Lambda] \tag{6-8}$$

where $[U]$ is the identity matrix, and $[\Lambda]$ is diag$\{\gamma_1, \gamma_2, ..., \gamma_n\}$. In a two-line coupled system, the propagation constants of the lines are given by

$$\gamma_1 = \sqrt{(Y_{11} + Y_{12})(Z_{11} + Z_{12})} \tag{6-9}$$

$$\gamma_2 = \sqrt{(Y_{11} - Y_{12})(Z_{11} - Z_{12})} \tag{6-10}$$

where γ_1 and γ_2 are propagation constants of eigenmodes, and similarly the characteristic impedance matrix which is defined as $[Z] = [S_v][S_i]^{-1}$ is

$$[Z] = \frac{1}{2}\begin{bmatrix} Z_1 + Z_2 & Z_1 - Z_2 \\ Z_1 - Z_2 & Z_1 + Z_2 \end{bmatrix} \tag{6-11}$$

where

$$Z_1 = \sqrt{\frac{Z_{11}+Z_{12}}{Y_{11}+Y_{12}}} \quad \textit{and} \quad Z_2 = \sqrt{\frac{Z_{11}-Z_{12}}{Y_{11}-Y_{12}}}\,.$$

Note, both propagation constant and characteristic impedance matrix have been represented by the series impedance matrix of (6-3) and parallel admittance matrix of (6-4).

In order to investigate the signal response of multiconductor interconnect circuits under arbitrary loading conditions the transfer functions must be found. The coupled interconnect line transfer functions under unmatched but special case terminal conditions have been reported in many papers [You90, Hwa91, Isa73, Ghi89].

A new transfer function for multiconductor coupled lines has been developed as a part of this research. Starting from the matrix equation (4-18) in Chapter 4, the coupled interconnect transfer function can be derived. The coupled line voltage eigenmatrix, $[S_v]$, and current eigenmatrix, $[S_i]$, in equation (4-18) were determined in Chapter 4 as equation (4-33) and equation (4-34), respectively. Since the constant matrix $[C_1]$ in (4-18) is the magnitude of an incident wave at launching port determined from boundary conditions,

$$[C_1] = \begin{bmatrix} V_1^+(x = 0) \\ V_2^+(x = 0) \end{bmatrix}. \tag{6-12}$$

Similarly, the constant matrix $[C_2]$ is the magnitude of a reflected wave at the launching port determined from boundary conditions. Thus,

$$[C_2] = \begin{bmatrix} V_1^-(x = 0) \\ V_2^-(x = 0) \end{bmatrix}. \tag{6-13}$$

Solving the matrix equation (4-18) with these eigenmatrices and boundary conditions, the transfer functions of coupled lines in the frequency domain including frequency variant line parameters and arbitrary loading conditions, i.e., $Z_{G1} \neq Z_{G2} \neq Z_{L1} \neq Z_{L2}$, are finally given by

$$H_1(\omega) = \frac{1}{det(A(\omega))} \{ T_1(\omega) + T_2(\omega) \} \tag{6-14}$$

$$H_2(\omega) = \frac{1}{det(A(\omega))} \{ T_1(\omega) - T_2(\omega) \} \tag{6-15}$$

where H_1 and H_2 are transfer function on line-1 (active line) and line-2 (quiet line), respectively and

$$T_1(\omega) = \{ Cof_{11}(A(\omega)) exp(-\gamma_1(\omega)x) + Cof_{13}(A(\omega)) exp(\gamma_1(\omega)x) \} \tag{6-16}$$

$$T_2(\omega) = \{ Cof_{12}(A(\omega)) exp(-\gamma_2(\omega)x) + Cof_{14}(A(\omega)) exp(\gamma_2(\omega)x) \} \tag{6-17}$$

where $Cof_{ij}(A)$ is the cofactor of square matrix $[A]$ which is given by

$$[A(\omega)] \equiv \begin{bmatrix} A_1(\omega) \\ A_2(\omega) \\ A_3(\omega) \\ A_4(\omega) \end{bmatrix} \tag{6-18}$$

where the respective row vectors of matrix $[A]$ are given by

$$[A_1(\omega)] = \begin{pmatrix} \left(\frac{Z_1(\omega)+Z_{G1}}{Z_1(\omega)}\right) & \left(\frac{Z_2(\omega)+Z_{G1}}{Z_2(\omega)}\right) & \left(\frac{Z_1(\omega)-Z_{G1}}{Z_1(\omega)}\right) & \left(\frac{Z_2(\omega)-Z_{G1}}{Z_2(\omega)}\right) \end{pmatrix}$$

$$[A_2(\omega)] = \begin{pmatrix} \left(\frac{Z_1(\omega)+Z_{G2}}{Z_1(\omega)}\right) & -\left(\frac{Z_2(\omega)+Z_{G2}}{Z_2(\omega)}\right) & \left(\frac{Z_1(\omega)-Z_{G2}}{Z_1(\omega)}\right) & -\left(\frac{Z_2(\omega)-Z_{G2}}{Z_2(\omega)}\right) \end{pmatrix}$$

$$[A_3(\omega)] = \begin{pmatrix} \left(\frac{Z_1(\omega)-Z_{L1}}{Z_1(\omega)}\right)\exp(-\gamma_1(\omega)l) & \left(\frac{Z_2(\omega)-Z_{L1}}{Z_2(\omega)}\right)\exp(-\gamma_2(\omega)l) \\ \left(\frac{Z_1(\omega)+Z_{L1}}{Z_1(\omega)}\right)\exp(\gamma_1(\omega)l) & \left(\frac{Z_2(\omega)+Z_{L1}}{Z_2(\omega)}\right)\exp(\gamma_2(\omega)l) \end{pmatrix}$$

$$[A_4(\omega)] = \begin{pmatrix} \left(\frac{Z_1(\omega)-Z_{L2}}{Z_1(\omega)}\right)\exp(-\gamma_1(\omega)l) & -\left(\frac{Z_2(\omega)-Z_{L2}}{Z_2(\omega)}\right)\exp(-\gamma_2(\omega)l) \\ \left(\frac{Z_1(\omega)+Z_{L2}}{Z_1(\omega)}\right)\exp(\gamma_1(\omega)l) & -\left(\frac{Z_2(\omega)+Z_{L2}}{Z_2(\omega)}\right)\exp(\gamma_2(\omega)l) \end{pmatrix}.$$

If $Z_{G1} = Z_{G2}$ and $Z_{L1} = Z_{L2}$ are assumed without considering frequency variant components, this equation reduces to formulas in the literature, previously shown in Chapter 4 [You90, Hwa91].

Given this generalized multiconductor interconnect transfer function in the frequency domain, (6-14) and (6-15), a method of time domain simulation needs to be developed. For an input pulse function which is excited in IC interconnect, the most stable method of pulse decomposition was used [Ika82]. Using this pulse decomposition method, the pulse with rise and fall time can be approximated as the summation of delayed unit step functions. The input function is

$$f(t) = \sum_{i=1}^{n} f_i(t) \qquad (6\text{-}19)$$

where

$$f_i(t) = \frac{A}{n}\left[U\left(t - \left(\frac{i-1}{n}\right)t_r\right) - U\left(t - \left(\frac{i-1}{n}\right)t_r - t_f\right)\right] \tag{6-20}$$

If interconnect line parameter matrices are known, the time domain responses of the interconnect under generalized conditions can be obtained by inverse Fourier transform of the above equation as

$$V_i(t\,,x) = \mathcal{F}^{-1}\left[F_i(\omega)H_i(\omega\,,x)\right] \tag{6-21}$$

where i is line number and x is distance.

This generalized multiconductor transfer function and Fourier transform technique were used for simulation of many types of multiconductor interconnect lines presented later in this chapter. A new algorithm (software) was developed for the simulations and the simulations were verified with picosecond pulsed measurements of interconnect lines.

6.3 Line Parameter Matrices for Simulations

The generalized interconnect transfer functions, (6-14) and (6-15) require knowledge of the multiconductor interconnect line circuit parameter matrices, $[R]$, $[L]$, $[C]$, and $[G]$, and terminal conditions of interconnect circuits, $[Z_G]$ and $[Z_L]$. The frequency dependent properties of the single conductor and multiconductor interconnect circuit models are discussed extensively in Chapter 4 and Chapter 5. The multiconductor line parameter matrices based on these results are reviewed below,

$$[\,R\,(\omega)] = \begin{bmatrix} R_{11}(\omega) & R_{12}(\omega) \\ R_{21}(\omega) & R_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} R_{11}(\omega) & 0 \\ 0 & R_{11}(\omega) \end{bmatrix} \tag{6-22}$$

$$[C(\omega)] = \begin{bmatrix} C_{11}(\omega) & -C_{12}(\omega) \\ -C_{21}(\omega) & C_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} C_{11}(\omega) & -C_{12} \\ -C_{12} & C_{11}(\omega) \end{bmatrix} \quad (6\text{-}23)$$

$$[G(\omega)] = \begin{bmatrix} G_{11}(\omega) & -G_{12}(\omega) \\ -G_{21}(\omega) & G_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} G_{11}(\omega) & 0 \\ 0 & G_{11}(\omega) \end{bmatrix} \quad (6\text{-}24)$$

$$[L(\omega)] = \begin{bmatrix} L_{11}(\omega) & L_{12}(\omega) \\ L_{21}(\omega) & L_{22}(\omega) \end{bmatrix} \approx \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{11} \end{bmatrix} \quad (6\text{-}25)$$

In the above parameter matrices, the components are composed of diagonal elements and off-diagonal elements. The diagonal parameters of the line parameter matrix are calculated from the single line interconnect frequency variant model [Eo92.a] (see Chapter 5). The coupling capacitance can be calculated by PISCES-IIB simulation [Tma90] or models [Sak83, Yua83, Che92]. Then, the coupling inductance is found via the free space capacitance matrix (see Chapter 4). The best methods of obtaining these interconnect circuit parameters are summarized in the next section.

6.4 Frequency Variant Circuit Parameter Models

This section reviews the equations useful for determining the interconnect circuit parameters for (6-22), (6-23), (6-24), and (6-25). These parameters are used in the generalized coupled interconnect transfer function, (6-14) and (6-15). These parameters are broken into three generic components. These are on-diagonal interconnect parameters (self-parameters), coupling capacitance parameters, and coupling inductance parameters.

6.4.1. Diagonal Interconnect Parameters

The interconnect cross section is composed of multiple dielectrics and its representative cross section is a sandwich structure of SiO_2 on a silicon substrate as shown in Fig. 3-2. From the interconnect cross section, parallel circuit parameters of interconnect are given from Chapter 5 by

$$G = \frac{\omega^2 C_1^2 G_s}{G_s^2 + \omega^2 (C_1 + C_2)^2} \tag{6-26}$$

$$C = \frac{\omega^2 C_1 C_2 (C_1 + C_2) + C_1 G_s^2}{G_s^2 + \omega^2 (C_1 + C_2)^2} . \tag{6-27}$$

where C_1 and C_2 are the oxide layer capacitance and silicon substrate capacitance, respectively and G_s is the conductance of the silicon substrate. Since fringing capacitance is in parallel with the above capacitance, the total capacitance becomes

$$C_T(\omega) = C(\omega) + C_f . \tag{6-28}$$

where C_f is the fringing capacitance,

$$C_f = \varepsilon \frac{2\pi}{ln\left[1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right]} \tag{6-29}$$

where ε is the double layered dielectric constant

$$\varepsilon = \frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2} \varepsilon_0 . \tag{6-30}$$

Here, the isolated conductor capacitance of (6-28) is related to the short-circuit capacitance which is defined in (6-5) (see Appendix B for a

discussion about definition of capacitance). That is, the short circuit self-capacitance becomes

$$C_{11}(\omega) = \frac{C_T(\omega) - 2C_{12} + \sqrt{C_T(\omega)^2 + 4C_{12}^2}}{2} + C_{12}. \qquad (6\text{-}31)$$

Note, the first term is the self capacitance under the coupled line and the second term is purely coupling capacitance. The modified resistance and inductance models that were derived in Chapter 5 are

$$R = \begin{cases} R_{dc} & ; if \quad R(f) < R_{dc} \\ R(f) = \dfrac{\rho}{\delta\left\{1 - exp(-\frac{t}{\delta})\right\}\left(1 + \frac{t}{w}\right)}\left(\frac{l}{w}\right) & ; if \quad R(f) > R_{dc} \end{cases} \qquad (6\text{-}32)$$

where

$$\delta = \frac{1}{\sqrt{\pi f \mu / \rho}}. \qquad (6\text{-}33)$$

The inductance is given by [Eo92.a]

$$L = \mu_0 \frac{1}{2\pi} ln\left[\left(\frac{h}{0.59w} + 1.1\right) - 0.5 + \sqrt{\left(\frac{h}{0.59w} + 1.1\right)^2 - 1.05}\right]. \qquad (6\text{-}34)$$

The above equations, (6-26) to (6-34), are used to determine the on-diagonal elements in (6-22) through (6-25).

6.4.2 Coupling Capacitance Matrix

The off-diagonal elements of (6-23) are determined using coupling capacitance expressions or simulations. Coupling parameters are

frequency variant. However, the frequency variant effects are small and can be neglected. The frequency dependence of the coupling capacitance is due to the frequency variant dielectric constant which is constant up to millimeter wave frequencies as discussed in section 5.4.2. Coupling capacitance is key to determining coupling noise. Since the space between lines is becoming narrower and narrower, exact knowledge of coupling capacitance in high speed VLSI circuit design is essential. There are many methods to calculate coupling capacitance. Currently, one of the approaches is numerical calculation [Wee70, Wei84, Nay89, Lio90] and the other is use of empirical expressions [Sak83, Yua82, Che92]. While numerical calculations take long times, they give more accurate capacitance values than empirical expressions. In contrast, the empirical expressions based on numerical calculation can be simple and closed form but are not as accurate as numerical calculations.

Below, coupling capacitance calculation using empirical expressions and numerical simulations are performed, followed by low frequency measurements in order to judge the best method for the finding coupling capacitance. A test structure for the coupling capacitance determination is shown in Fig. 6-1 and its cross section is shown in Fig. 6-2. The test structures are 1 cm long and have variable line widths (2 and 4 μm) and line spacings (2 and 4 μm). To allows two port network measurements, each line has only one pad and the pads are located on opposite sides of the structure.

A. Empirical Expression: In many VLSI circuit designs or simulations, empirical expressions for coupling capacitance are usually

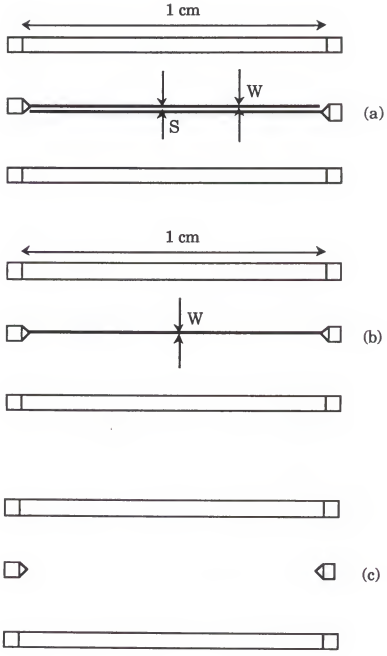


Fig. 6-1 Cross coupled interconnect test structure layout.
(a) Cross coupled test structure.
(b) Single line test structure.
(c) Open of the test structure.

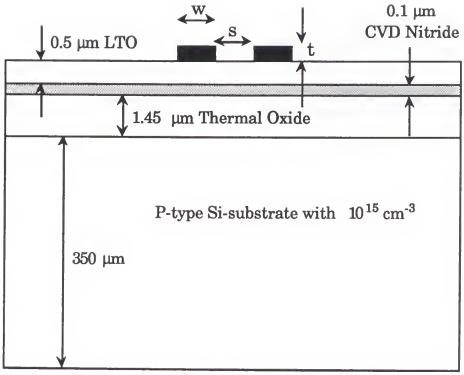


Fig. 6-2 Test structure cross section.

used because of their simplicity and short calculation time. Most of these expressions are represented by a configuration-based aspect ratio, i.e., the combination of conductor thickness, t, and its width, w, dielectric material height, h, and between line space s. There are several well known expressions. The first one is given by [Sak83]

$$C_{12} = \varepsilon_{ox}\left\{ 2.80\left(\frac{t}{h}\right)^{0.222}\left[\left(\frac{s}{h}\right)^{-1.34}\left(0.03\left(\frac{w}{h}\right) + 0.83\left(\frac{t}{h}\right) - 0.07\left(\frac{t}{h}\right)^{0.222}\right)\right]\right\}. \qquad (6\text{-}35)$$

This expression is not accurate when compared with PISCES-IIB numerical simulation as shown in Table 6-1. The second, the curve fitting expression using "least square fit" methods based on numerical calculation from [Yua82] is given,

$$C_{12} = \varepsilon_{ox}\left\{ 0.0046\left(\frac{w}{h}\right)^{1.67} + 0.0271\left(\frac{h}{t}\right)^{1.56} + \left(\frac{s}{t}\right)^{-1.057}\left[0.496\left(\frac{w}{t}\right)^{0.248} + 0.914\left(\frac{h}{t}\right)^{0.203}\right]\right\} \qquad (6\text{-}36)$$

This is better than (6-35). However, it gives accurate coupling capacitance with moderate space between lines (see Table 6-1) . In general, (6-36) not only overestimates capacitance for the narrow spacing, but underestimates capacitance for wide strips. Finally, an empirical expression is given recently [Che92],

$$C_{12} = \varepsilon_{ox}\left\{ 1.064\left(\frac{t}{s}\right)\left(\frac{t+2h}{t+2h+0.5s}\right)^{0.695} + \left(\frac{w}{w+0.8s}\right)^{1.4148}\left(\frac{t+2h}{t+2h+0.5s}\right)^{0.804} + 0.831\left(\frac{w}{w+0.8s}\right)^{0.055}\left(\frac{2h}{2h+0.5s}\right)^{3.542}\right\} \qquad (6\text{-}37)$$

Table 6-1 Coupling capacitance from various characterization methods. Unit of capacitances is pF/cm. Parentheses of columns 3 and 4 mean self capacitance.

W (μm)	S (μm)	measure (C_{11})	PISCES-II	exp. (35) (Saku.)	exp. (36) (Yuan)	exp. (37) (Chern)
2	2	0.3095 (0.7095)	0.362 (0.852)	0.313	0.303	0.421
2	4	0.1316 (0.8113)	0.1492 (0.957)	0.123	0.162	0.208
4	2	0.3375 (1.0315)	0.368 (1.191)	0.336	0.325	0.478
4	2	0.1885 (1.1115)	0.151 (1.297)	0.133	0.174	0.256

Since this expression uses many weighting factors for its formulation, its deviation from numerical calculations is small. These closed form expressions are suitable for CAD program subroutines, however, numerical simulation is required for the highest accuracy.

Table 6-1 shows the capacitances of coupled interconnects from various characterization methods. The measured capacitance at low frequency, C_{11}, the capacitance from PISCES-IIB simulation, the capacitance from (6-35), the capacitance from (6-36), and the capacitance from (6-37) are presented. The author finds that the capacitances from PISCES-IIB simulation agree with measurements over a wide range of structures.

B. Numerical Simulation of Coupling Capacitance (PISCES-IIB Simulation): Among many numerical capacitance calculation methods, the PISCES-IIB [Tma90] is an excellent tool to determine capacitance as discussed in Chapter 2 [Eo90]. It not only solves all the semiconductor equations, i.e., Poisson's equation and continuity equations but can be readily applied to complex thin film structures such as sandwiches of multilayered dielectric materials. PISCES-IIB AC simulation yields parallel admittance parameters such as conductance and capacitance matrices. The conductance value which is of lesser importance is not in good agreement with experimental values. Its divergence at high frequency is a problem. However, capacitance calculation with PISCES-IIB simulation of single interconnect lines up to moderate frequency shows excellent agreements with s-parameter measurements (see Chapter 3 and Chapter 5) [Eis92, Eo90]. Since IC interconnect lines are separated only by SiO_2, whose properties are relatively independent of

frequency, coupling between lines is virtually independent of frequency. Thus, accurate coupling capacitance calculation can be achieved with PISCES-IIB simulations at low frequencies.

C. Low Frequency Measurements: The best test of the various coupling capacitance expressions and numerical simulations is comparison with measurements. Low frequency capacitance measurements were performed using short circuit measurement techniques for the test structure shown in Fig. 6-1 [Wee70, Lin90a, Lin90b]. A cross section of the test structure is shown in Fig. 6-2. Open pad measurements were used to de-embed the pad parasitics.

Coupling capacitances from all the capacitance characterizations including the measured low frequency capacitances are tabulated as Table. 6-1. Simulations and empirical expressions have been done with space variation from 0.1 μm to 10 μm. PISCES-IIB simulations show excellent agreement with measurements as is expected. From the Table 6-1 expression (6-36) agrees fairly well with the PISCES-IIB simulation results and low frequency measurements. However, the empirical models show significant deviations for narrow spaces between lines. The deviation of the empirical model from experimental values occurs because the empirical model does not include silicon substrate effects. It must be emphasized here that the coupling capacitances drastically increase as the line space is narrowed. This research indicates that the PISCES-IIB simulations are the best method of determining the coupling capacitance C_{12} for the interconnect circuit parameter matrix (6-23).

6.4.3. Coupling Inductance Matrix

The final elements that must be determined in are the interconnect circuit parameter matrix off-diagonal inductance elements. These are inserted in (6-25) and used for the coupled interconnect circuit simulations with the generalized transfer function.

At low frequencies, inductance is not a dominant IC interconnect coupling parameter. However, as line-widths become finer and frequency increases, inductance becomes increasingly important. Moreover, the field effect of the magnetic coupling has a larger range than that of the capacitive coupling [Yua82a]. The inductive coupling coefficient matrix can be determined from the free space capacitance matrix if the interconnect is a lossless or a low loss line. That is, the capacitance and inductance for lossless line are related by [Mat69, Fra77],

$$[L][C_o] = \frac{1}{v^2}[U] = \mu_o \varepsilon_o [U] \tag{6-38}$$

where "v" is the wave propagation velocity, $[U]$ is an identity matrix, and $[C_o]$ is the free space capacitance matrix. However, inductance matrix calculation for lossy lines is intractable and cannot be determined simply from (6-38). The silicon substrate conductance as well as transmission line resistance are not negligible at high frequencies. Besides, even at low frequencies the metal interconnect resistance is not negligible for modern fine line interconnect. Thus, the simple expression of (6-38) must be modified. Introducing a parameter, $\hat{\varepsilon}_r$, which is a small perturbation for lossy effects, the inductance matrix is expressed by

$$[\,L\,] = \hat{\varepsilon}_r \begin{bmatrix} \mu_o\varepsilon_o & 0 \\ 0 & \mu_o\varepsilon_o \end{bmatrix} [C_o]^{-1}, \tag{6-39}$$

where $\hat{\varepsilon}_r$ is determined from the single interconnect line model or single line measurements as in Chapter 4. Letting the single line inductance be L_s, $\hat{\varepsilon}_r$ becomes

$$\hat{\varepsilon}_r = \frac{L_s C_{so}}{\mu_o \varepsilon_o} \tag{6-40}$$

where C_{so} is the single-line capacitance for free space. Measurements show that the above inductance expressions vary weakly with frequency. Thus, the high frequency inductance value is very close to the low frequency one as shown in Chapter 5. Therefore, it is possible to use low frequency inductance values determined by (6-39) at high frequencies and retain good accuracy in the generalized interconnect transfer function.

6.5 Signal Transient, Propagation, and Crosstalk Simulation

6.5.1 Simulation Strategy

Now that the generalized multiconductor interconnect transfer function and the interconnect circuit parameters have been determined it is possible to do time domain simulation of interconnect circuit response. This section presents interconnect circuits and the algorithm used to investigate multiconductor interconnect circuit signal response.

Interconnect circuit models, loading conditions, and the space between interconnect lines are varied to investigate interconnect signal variation. First, interconnect time-domain circuit responses with the

frequency variant model are compared with existing interconnect models such as RC, LC, and RLC models. Various loading conditions are used for the simulations since loading conditions greatly affect the response. Finally, the effects of line spacings are shown since line spacing is a primary factor in signal coupling.

A coupled interconnect circuit is shown in Fig. 6-3. Input signal, V_i, is applied to input impedance, Z_{Gi}, at line-1 as in Fig. 6-3. The pulse width of the input signal, t_w, and its rise time, t_r, are 500 ps and 30 ps, respectively, as shown in Fig. 6-4. The test structure has metal lines on SiO_2-nitride-SiO_2 on a silicon substrate as in Fig. 6-2. The interconnect line width is 4 μm and its thickness is 1 μm. The length of the line is 1 cm. The interline space is varied from 0.5 μm to 10 μm. The doping concentration of the silicon substrate is assumed to be uniform $1x10^{15}$ cm^{-3} p-type.

The generalized interconnect transfer function simulation algorithm is conceptually described in Fig. 6-5 with structured programming language. The main procedure of the algorithm is composed of subprocedures and several blocks which are represented by bold face characters in Fig. 6-5. The procedure and subprocedures are a complete module that perform an independent function and produce outputs with given inputs, while the blocks are dependent functional unit because it use global data. The functions of the respective procedures and their input-output relationships are as follows:

INCT_SIMULATION : main procedure

input : interconnect dimensions and processing parameters

output : time domain response of the interconnect circuits.

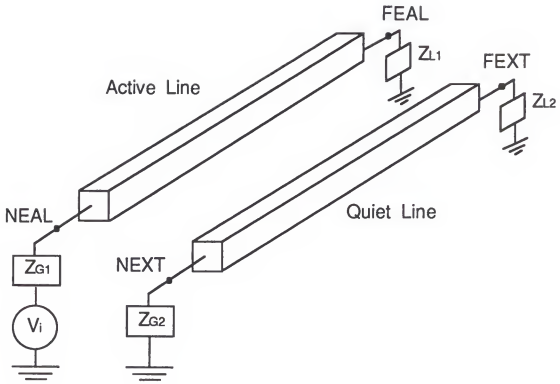
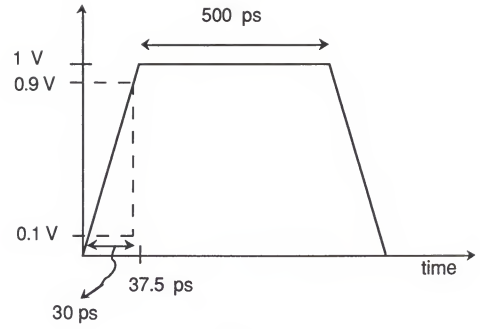
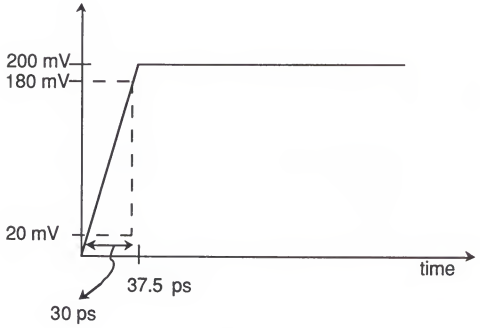


Fig. 6-3 Interconnect circuits and test points.



(a)



(b)

Fig. 6-4 Input pulse.
(a) Step pulse (for simulations).
(b) Unit step pulse (for measurements).

```
Procedure INCT_SIMULATION (input, output)
{
begin
      INPUT_FT // input function Fourier transform block. //
      for nodenum (1:n)
            for fstep (0:n)
                  TRAN_FT  // frequency domain output
                           calculation block //
                        {
                        Procedure PARAMETER (input, output)
                        Procedure WAVE_CONDITION (input, output)
                        F_RESPONSE     // block to calculate frequency
                                       response //
                        }
            endfor_fstep
            for tstep (0:n)
                  T_RESPONSE     // inverse fourier transform block //
            endfor_tstep
      endfor_nodenum
      PLOTTING        // output representation block //
endbegin
}
```

Fig. 6-5 Simulation algorithm of coupled interconnects.

PARAMETER : subprocedure to calculate line parameter matrices

input : interconnect dimensions and processing parameters

output : line parameter matrices.WAVE_CONDITION : subprocedure to calculate wave parameters

input : line parameter matrices

output : matching conditions, propagation constants, and characteristic impedances.

The function of the blocks entitled INPUT_FT, TRAN_FT, T_RESPONSE, and PLOTTING are described in Fig. 6-5 with double backslash. The algorithm has been implemented in FORTRAN-77 on a SUN-SPARC workstation.

6.5.2 Simulation Models

In this work, simulations using a new generalized frequency variant RLCG model as well as RC, RLC, and lossless LC models have been performed. These models have the following properties.

A. RC model: Standard VLSI designs use this simple model. The simple form is suitable for CAD subroutines. However, it gives incorrect crosstalk noise estimation as well as inaccurate signal delay at high frequency. Thus, it is not appropriate for the highest speed VLSI circuit design.

B. LC model: The lossless LC model is acceptable for wide and thick interconnect. Such assumptions are valid for IC packages and PC boards but not for on-chip interconnect. Reflection and coupling noise are

overestimated on this model. Lossy models have to be incorporated for exact prediction of the on-chip interconnect characteristics. However, the LC model provides a upper bound for lossy crosstalk.

C. RLC (constant) model: This model combines elements from the previous two models. It may be a good approximate model for upper-level metal up to hundreds of MHz frequencies. However, when the frequency is very high, it requires more accurate models are needed to predict accurate rise time, fall time, and crosstalk noise. Crosstalk effects of the coupling inductance operate over long ranges. Crosstalk due to the inductance of a close line spacing (large mutual inductance) with a capacitive load can be predicted well with this constant RLC model. A crosstalk of a wide line spacing (small mutual inductance) or resistive loads are predicted poorly with this model.

D. Generalized RLCG (frequency variant) model: This is a new model developed in this work (see Chapter 3 and Chapter 5). It is the most accurate model and is necessary for the highest performance digital VLSI circuit design. In this model, all the interconnect circuit parameters can vary with frequency.

The characteristics of the above models are compared and summarized at Table 6-2.

6.5.3 Simulation Results

In the multiconductor interconnect circuit the signal test points are $V_1(t, 0)$, $V_2(t, 0)$, $V_1(t, l)$, and $V_2(t, l)$ in Fig. 6-3. The acronyms used in

Table 6-2 Attributes of various interconnect models.

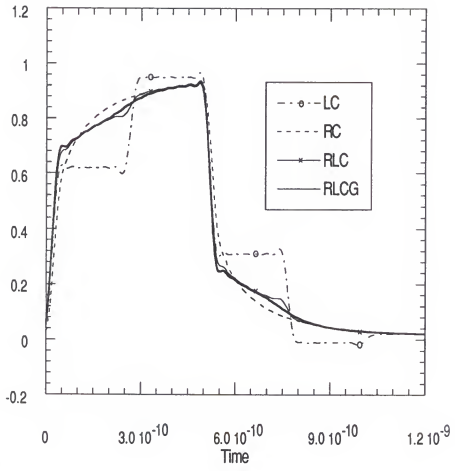
items / models	properties	comments
RC	- simple, but inaccurate predition of all the circuit responses such as rise and fall time, crosstalk noise.	- widely used. - used for simple efficient CAD model.
RLC	- only acceptible for wide and thick interconnect up to moderate frequency. - inaccurate prediction of circuit responses for high performance VLSI.	- good approximate model for first level metal.
LC	- lot of reflections. - upper bound of the crosstalk noise - does not attenuate the ripple signal.	- only acceptible for off-chip or package interconnect. - not suitable for on-chip interconnect.
RLCG (ω)	- can explain frequency varient propeties of interconnect parameters. - skin effect and dielectric loss are incorporated. - exact prediction of signal variations.	- the most general model. - suitable for high performance VLSI circuit design. - numerically inefficient

Fig. 6-3 are in order, signal detected at the near end of the activated line (NEAL), near end crosstalk (NEXT), signal detected at the far end activated line (FEAL), and far end crosstalk (FEXT). These are the signal nodes in the interconnect circuit simulations.

Time domain simulation shows signal transient, propagation, and crosstalk at these four test nodes of coupled interconnect circuits with termination impedances as defined in Fig. 6-3. Given a input signal applied at V_i, signal transients can be observed in the four test points. Propagation delay and signal degradation can be observed in the test point, FEAL. The NEXT and FEXT show crosstalk at the quiet line. Both near end crosstalk and far end crosstalk signals may become undesirable inputs signal for neighbor gates or stages. This is a major cause of circuit malfunction. Since signal coupling is inversely proportional to spacing between two lines, the exact characterization of the crosstalk noise important for high density VLSI circuit design. The simulation results are shown in Figs. 6-6 through 6-8.

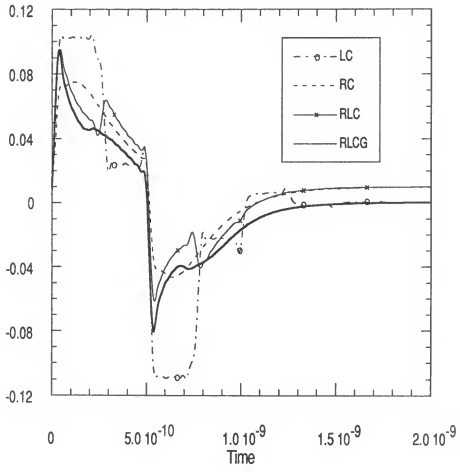
In these figures, the heavy solid lines represent the frequency variant RLCG model. The RLCG model is the most accurate, so other models are judged relative to this model. Note that the all the input and output impedances are represented as pairs of resistance and capacitance, Z_{Xi} = (resistance, capacitance).

First, Fig. 6-6 shows the effects of frequency variant line parameters where input impedances are $Z_{G1} = Z_{G2}$ = (50 Ω, 0pF) and the load impedances are $Z_{L1} = Z_{L2}$ = (500 Ω, 0.1pF). Fig. 6-6-(a) shows a signal transient at the near end of active line (NEAL). Here all the other models show similar signal variations except the LC model. The LC model gives

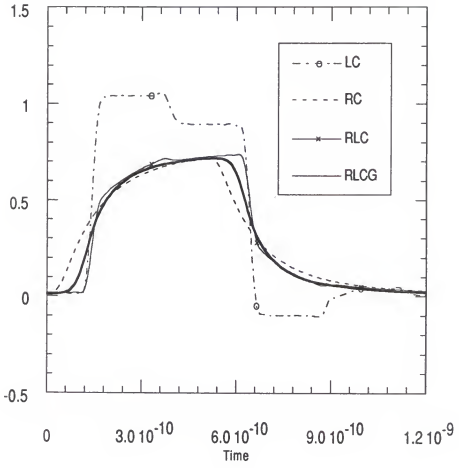


(a) at NEAL (Near End Active Line).

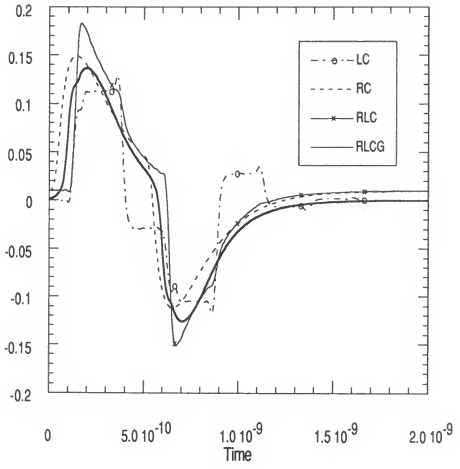
Fig. 6-6 Comparison of various interconnect line parameter models. Heavy solid line is the most accurate frequency variant RLCG model.



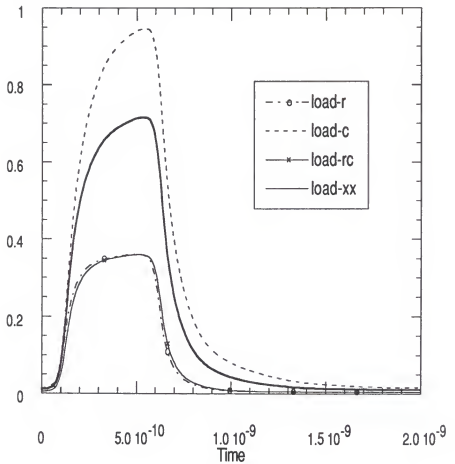
(b) at NEXT (Near End Cross(X)Talk).
Fig. 6-6--continued.



(c) at FEAL (Far End Active Line).
Fig. 6-6--continued.

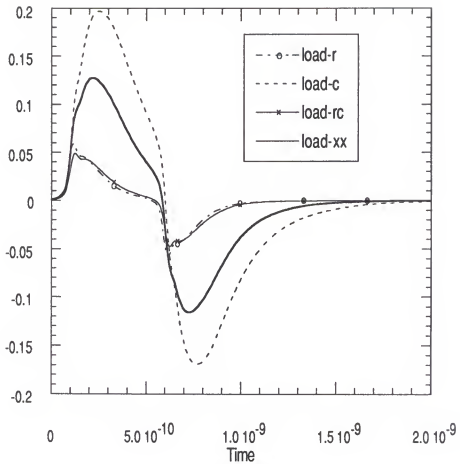


(d) at FEXT (Far End Cross(X)Talk).
Fig. 6-6--continued.

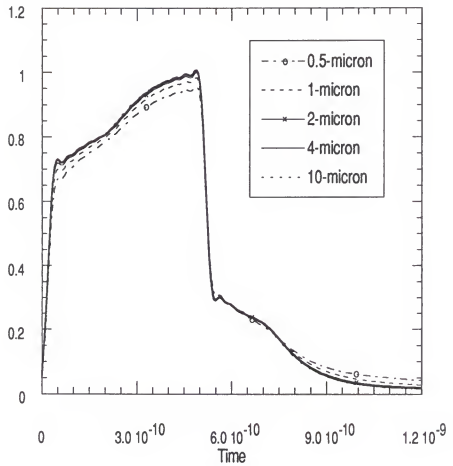


(a) at FEAL.

Fig. 6-7 Interconnect response with differing loading conditions. In the legend r means resistance and c means capacitance.

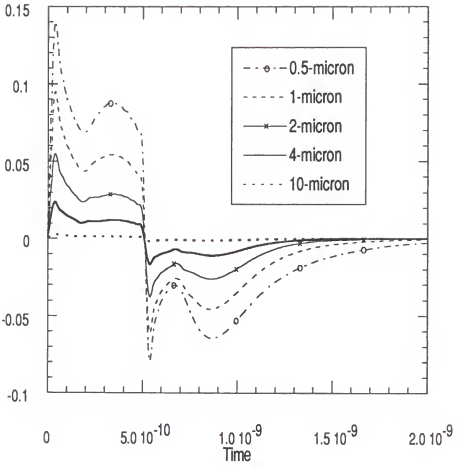


(b) at FEXT.
Fig. 6-7--continued

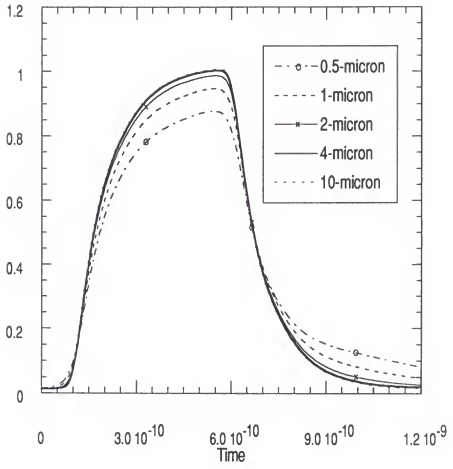


(a) at NEAL.

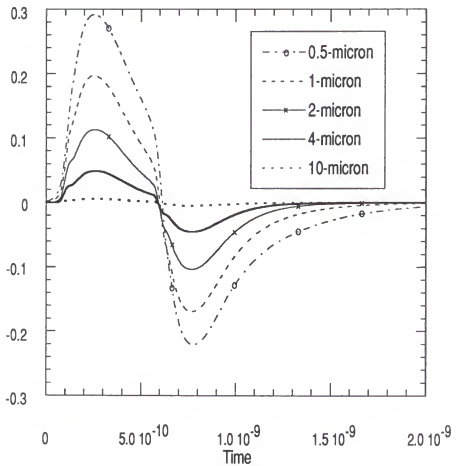
Fig. 6-8 Comparison of interconnect line spacing effects with frequency variant RLCG models.



(b) at NEXT.
Fig. 6-8--continued



(c) at FEAL.
Fig. 6-8--continued



(d) at FEXT.

Fig. 6-8--continued

features not present in the real interconnect transients. Fig. 6-6-(b) shows near end crosstalk at the near end of the quiet line (NEXT) at 1 μm line space. Note, the RC model and the LC model show inaccurate signal crosstalk at this point. That is, the RC model underestimates the magnitude of signal coupling by 21 %, while the LC model overestimates the magnitude of signal coupling by 10 %. Fig. 6-6-(c) shows signal delay and degradation at the far end of the active line (FEAL). The LC model gives highly inaccurate predictions of wave shape and magnitude. The RC model underestimates and the RLC model overestimates by about 50 ps the delay as compared to the frequency variant RLCG model. This is about 33 % error. Moreover, the RC model inaccurately underestimates rise and fall times, while the RLC model overestimates them. Fig. 6-6-(d) shows crosstalk noise at the far end of the quiet line (FEXT). The RC model overestimates the magnitude by 15 % and signal delay of RC model is underestimated by 50 ps. This is about 50 % error. Note that RC model underestimates the magnitude of the near end crosstalk by 21 %. Now, it is very clear from Fig. 6-6 that the RC model and LC model cannot predict the precise signal delay or crosstalk. Although the RLC model can be a good approximate model, it can underestimate or overestimate crosstalk noise. The RLC model also shows a moderately inaccurate prediction of the signal delay, rise time, and fall time. Moreover, in future VLSI circuits, since average interconnect length will become longer and line spaces will become even narrower, inaccuracies in the RC and RLC models will become more significant.

In summary, existing interconnect circuit models underestimate signal magnitude and delay in some cases and overestimate it in other cases. For example, the RC model underestimates near end crosstalk

noise, but it overestimates far end crosstalk. Such discrepancies will increase as circuit density and circuit speed increases. Thus, the use of existing models for high speed circuit design will become riskier in the near future. The remaining simulation work of this dissertation employs the frequency variant RLCG model to explore signal transmission in ICs and verify simulations with measurements.

Simulations of four different load circuits are performed since different loading conditions also cause different signal variations. Simulations of a capacitive load (load-c in Fig. 6-7) typical of a CMOS gate (0 Ω, 0.2 pF), a combination of capacitance and resistance loads (load-rc and load-xx in Fig. 6-7) typical of a BJT base input of (500 Ω, 0.2 pF) or (100 Ω, 0.2 pF), and a resistive load (load-r in Fig. 6-7) typical microwave circuit load (100 Ω, 0 pF), have been performed. The CMOS like capacitive load (0 Ω, 0.2 pF) simulations show the magnitude of a pulse is maintained while its crosstalk becomes much higher than that of a resistive load (100 Ω, 0 pF). From these simulations, it can be also seen that the capacitive load makes pulses become wider. Moreover, capacitively loaded circuits must be more carefully designed considering the increased crosstalk noise. The BJT loads exhibit behavior that has features of both the capacitive and resistive loads.

Finally, line spacing effects are shown in Fig. 6-8. Here, the interconnect loads are assumed capacitive (CMOS) and the line spacing is varied from 0.5 μ to 10 μ. As the line spacing becomes narrower, coupling noise is drastically increased. In Fig. 6-8-(a), the effects of line spacing at the near end of the active line are shown. At node NEAL, the effects are not significant, but narrowing the spacing between two lines with the same

line width reduces the magnitude of pulse. Fig. 6-8-(b) shows the near end signal coupling. As line spacing is narrowed to submicrometer dimensions, coupling is greatly increased. Signal delay and waveform degradation at far end of active line are shown in Fig. 6-8-(c). Significant reduction of transmitted pulse magnitudes are observed for narrow line spaces. The average length of interconnect line becomes longer as integration level increases. Thus, higher density circuit design faces serious waveform degradation problems. Far end crosstalk effects due to line space are shown in Fig. 6-8-(d). The far end crosstalk with narrow line spacing is very significant and happens after some delay. For example, 0.5 micron line space shows 30 % coupled signal magnitude as compared to launched signal magnitude. For 5 V power supply this is a coupled signal value of 1.5 V which is enough to activate a gate on an adjacent quiet line. Such interconnect effects may be catastrophic because these will occur unexpectedly and intermittently. Therefore, as line spaces become narrower and length becomes longer, poor interconnect models could result in design failures or excessive die area.

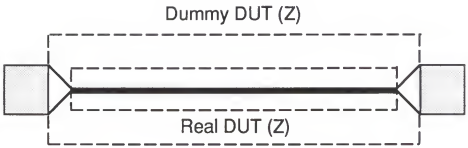
One of the major problems that high speed circuit modelers have not solved accurately is crosstalk noise. Thus, worst case design rules must be used. This causes an increase in interconnect spacing and occupation of the die area. Thus the level of integration becomes restricted. Such restrictions will become much more severe as the line spacing is reduced. Note, these simulations show signal coupling due only to one active line. In real circuits, there are many signal lines near a interconnect line. These signal lines cause signal coupling with each other. Thus, the coupled signals which are superposed on the interconnect become much larger than two interconnect line coupling.

6.6 Experimental Verification in Time Domain

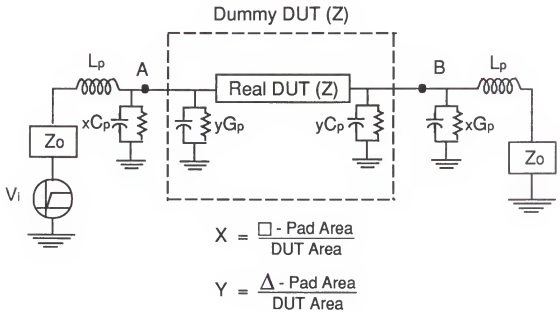
The coupled interconnect circuit simulations that employ generalized interconnect transfer function, i.e., (6-14) and (6-15), and frequency variant interconnect circuit parameter model (frequency variant RLCG model) are verified using picosecond time domain measurements in this section.

In order to perform measurements of interconnect signal variations in the time domain, the test structures shown in Fig. 6-1 were designed. The line widths are 2, 4, and 10 μm for single-lines and 2 and 4 μm for the cross-coupled lines. The slot widths of the cross-coupled lines are 2 and 4 μm. They are fabricated over a SiO_2 layer, a thin film nitride layer, and a P-type Si-substrate with the concentration of 10^{15} cm^{-3}. For the time domain measurements a HP54121T sampling oscilloscope is connected to the Cascade Microtech Probe Station and the DUT is mounted on the measurement chuck. The termination condition of the measurement system is internally 50 Ω at the measurement points. In time domain measurements, it is difficult to eliminate the pad parasitic effects. Thus, it is impossible to predict exact circuit parameters only from time domain measurements. It is necessary to model the IC pad response and add it to the interconnect circuit response. This difficulty is inherent in time-domain measurements. Moreover, pad parasitics also show frequency variant effects in high frequency.

Equivalent circuits of the measurement system including DUT and pad parasitics are shown in Fig. 6-9. In these simulation circuits, the pad



(a)

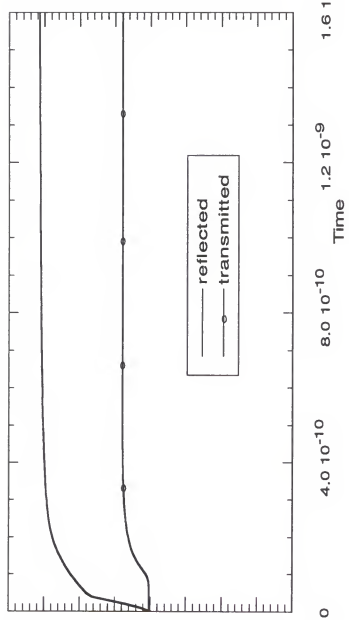


(b)

Fig. 6-9 Simulation circuits of the test structure.
(a) Test structure. (b) Equivalent circuit model.

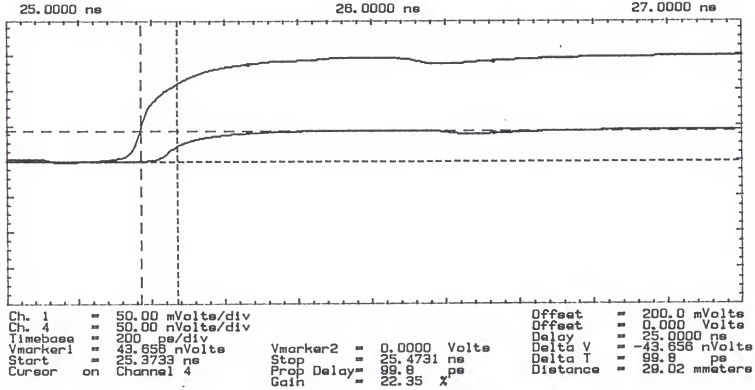
parasitics are divided into two parts. Their frequency dependencies are calculated by using proportional factors, x and y. They are the ratios of the areas (i.e., pad area) to DUT area. Parasitic inductance values are in the range of 0.3 nH to 0.5 nH. In this simulation, L_p is assumed to be 0.5 nH. In the single line measurements, signal transients and signal propagation at the NEAL and FEAL can be observed. The two port network measurements make it possible to observe the FEXT from the cross-coupled structure. Thus, if floating terminals of the DUT are assumed to have very high resistance such as 1 MΩ, then the simulation is easily done. Since the internally generated input function of the HP54121T sampling oscilloscope is a unit step [Hp90], measurement results can be compared with the simulation results under the same conditions. As expected from simulation, signal is delayed and dispersed, and there is crosstalk noise due to coupling.

The comparisons of the simulated and experimental results for single-line interconnect are shown in Fig. 6-10. Fig. 6-10-(a) and Fig. 6-10-(b) show a simulation and a measurement for a 2 μm wide single line, respectively. The simulation shows excellent agreement with experimental data in magnitude, delay, and waveform. Similar simulation and experiments for single line with different line widths have been shown in Fig. 6-10-(c) to Fig. 6-10-(f). Fig. 6-10-(c) and Fig. 6-10-(d) show results for 4 μm width interconnect. Fig. 6-10-(e) and Fig. 6-10-(f) show results for 10 μm wide interconnect. The single line simulation and experiments verify that the response of interconnect can be accurately predicted by the frequency variant RLCG model.



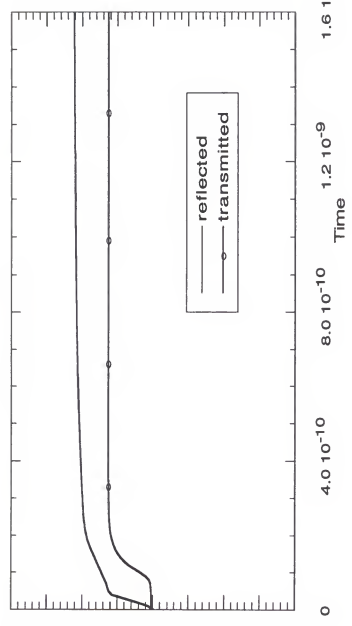
(a) Simulated reflection signal of 2 μm line width at NEAL and transmission signal at FEAL.

Fig. 6-10 Simulated and measured signals of single line.



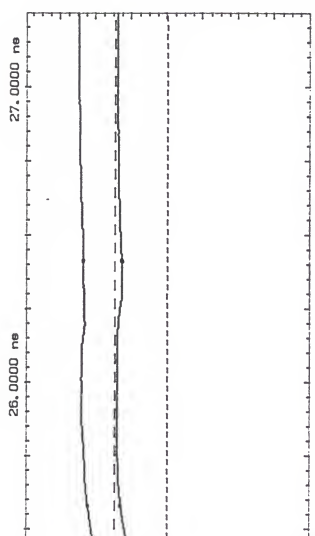
(b) Measured reflection signal of 2 μm line width at NEAL and transmission signal at FEAL.

Fig. 6-10--continued.



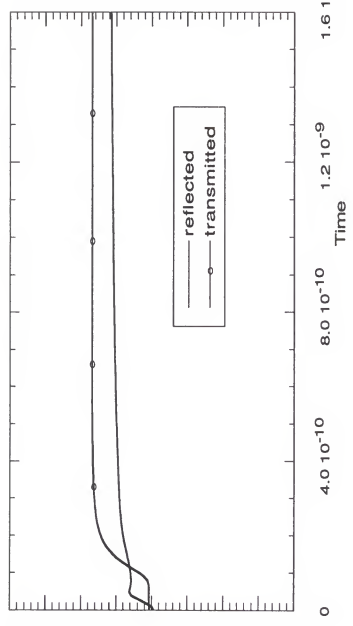
(c) Simulated reflection signal of 4 μm line width at NEAL and transmission signal at FEAL.

Fig. 6-10--continued.



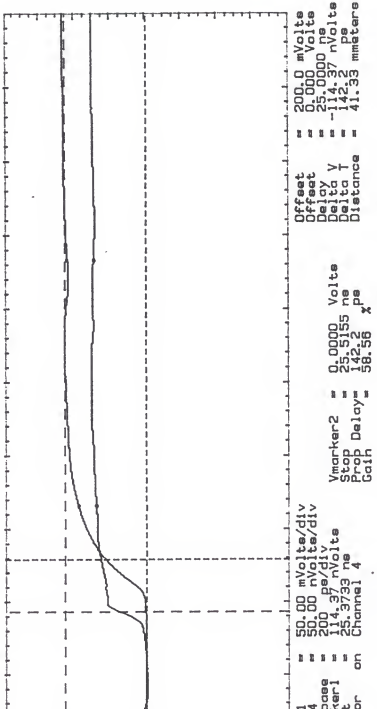
(d) Measured reflection signal of 4 μm line width at NEAL and transmission signal at FEAL.

Fig. 6-10--continued.



(e) Simulated reflection signal of 10 μm line width at NEAL and transmission signal at FEAL.

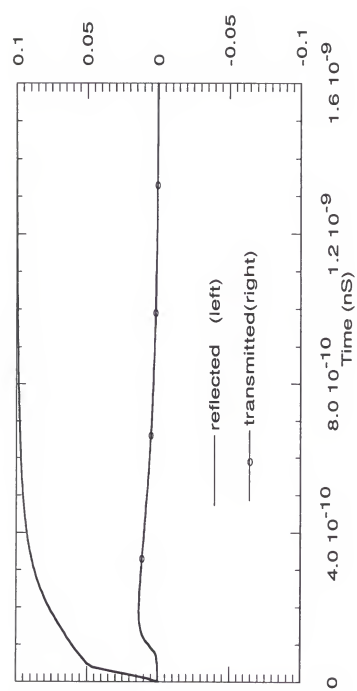
Fig. 6-10--continued.



(f) Measured reflection signal of 10 μm line width at NEAL and transmission signal at FEAL.

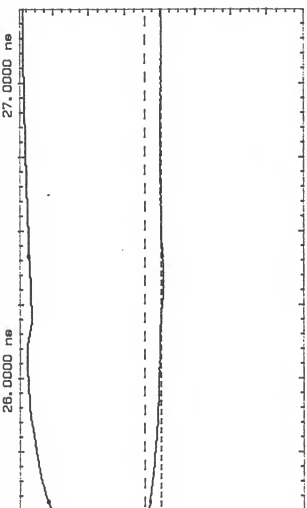
Fig. 6-10--continued.

Fig. 6-11 shows time domain simulation and measurement results for coupled lines. Fig. 6-11-(a) shows simulated reflected signal transients for near end and far end crosstalk of a quiet line (FEXT). Fig. 6-11-(b) shows time domain measurements of the reflected signal transients and crosstalk for the far end of the quiet line (FEXT). Interconnect with 2 μm line width and 2 μm line spacing was used and the cross sections are the same as in Fig. 6-2. The simulation employed the frequency variant RLCG model for diagonal element determination of transmission line circuit parameter matrices. In order to calculate coupling capacitance, PISCES-IIB simulation was performed. The inductance matrix was calculated from (4-60). The excellent agreement between simulation and time domain measurements verify that the frequency variant RLCG model is the most accurate model and that resistive and conductive coupling are not the dominant coupling mechanisms. Thus, the validity of the assumptions that are used for the simplified coupling parameter extraction in Chapter 4 are proven by these simulations and experiments. Similar simulations and experiments for other cross coupled lines (4 μm wide lines and 2 μm line spacings and 4 μm line wide and 4 μm line spacings) have been shown in Fig. 6-11-(c) to Fig. 6-11-(f). These simulation and measurement results demonstrate that the frequency variant RLCG model is an excellent model for high performance VLSI circuit design. The important signal transmission features for the interconnect circuit simulation and measurements are compared in Table 6-3. The agreement is very good. Sources of error include the simplified parameter extraction methodology, time domain measurement error, and the pad parasitic response model.



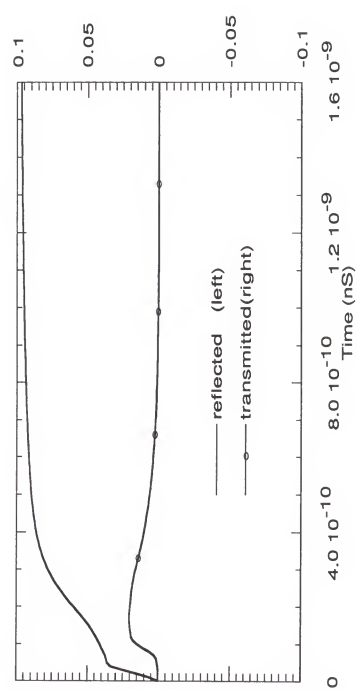
(a) Simulated reflection signal of 2 μm line width and 2 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11 Simulated and measured signals of cross coupled lines.



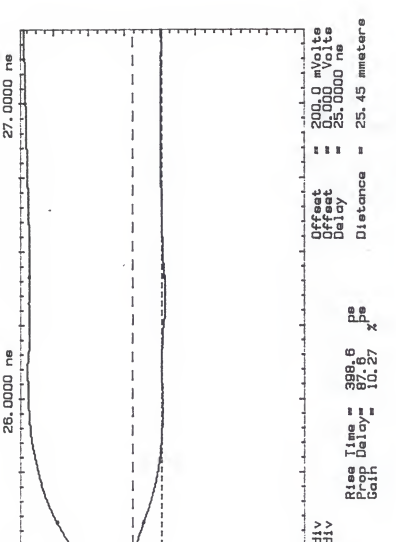
(b) Measured reflection signal of 2 μm line width and 2 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11--continued.



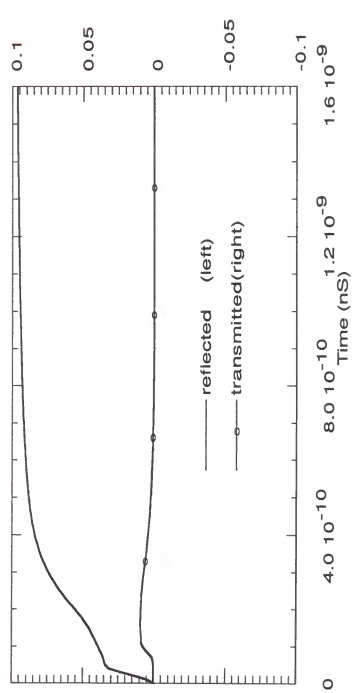
(c) Simulated reflection signal of 4 μm line width and 2 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11-continued.



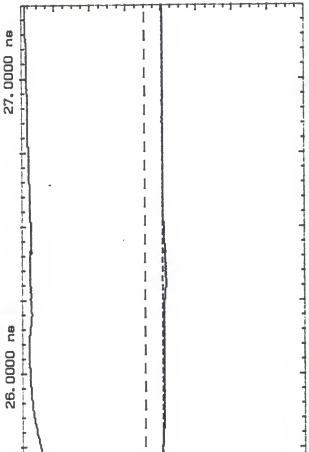
(d) Measured reflection signal of 4 μm line width and 2 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11--continued.



(e) Simulated reflection signal of 4 μm line width and 4 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11--continued.



(f) Measured reflection signal of 4 μm line width and 4 μm line space at NEAL and transmission signal at FEXT.

Fig. 6-11--continued.

Table 6-3 Comparison of simulated and measured circuit parameters.

ITEM *			propagation delay (ps)		peak value (mV) at NEAL		peak value (mV) at FEAL or FEXT	
line	W	S	simu.	meas.	simu.	meas.	simu.	meas.
SG	2	x	100	99.8	160	150	40	43.75
SG	4	x	100	109.7	110	125	60	68.75
SG	10	x	100	142.2	85	112.5	60	75
CC	2	2	75	72.9	200	200	12.5	12.5
CC	4	2	75	87.6	200	200	20	18.75
CC	4	4	87.5	89.4	200	200	10	12.5

* SG: single line.
CC: cross coupled lines.
W: line width.
S: space between lines.

This dissertation shows that experimental measurements of interconnect signal transmission can be predicted by the frequency variant RLCG model and the new generalized interconnect transfer function. That is, signal transient, crosstalk noise, and delay, which are essential information for IC circuit designs, can be precisely predicted. The interconnect simulation can with minor modifications include high frequency parasitic effects. These effects are hard to independently observe using existing time domain experimental tools.

6.7 Summary and Discussion

Through an exact mathematical analysis, the generalized interconnect transfer functions are derived. Using frequency variant parameter modeling of coupled interconnect, high speed VLSI interconnect simulations have been performed. To verify these theoretical analyses, computer simulation and experiments in the time domain have been performed.

Many published papers have assumed a single-dielectric of SiO_2 which is acceptable only for MCMs (Multi-Chip Module) on silicon. However, a new generalized model removing these simplifying assumptions of previous work has been developed. Existing models of VLSI interconnect have been compared in this work (RC, LC, RLC, and frequency variant RLCG models of interconnect line). These models were used for the simulations of the time domain responses. The discrepancies and inaccuracies of the various models have been shown through these models and simulations. The results of these simulations show that the

exact rise and fall time as well as very accurate crosstalk can be predicted from the frequency variant interconnect models.

Test structures with single and cross-coupled lines were designed, and time domain measurements were performed with a high speed sampling oscilloscope, HP54121T. The experimental results were compared with the frequency variant RLCG simulation results under various conditions. They showed excellent agreement. Furthermore, the effects of pad parasitics, which can not be avoided during time-domain measurements were characterized with this simulation methodology.

The most important results in this Chapter are summarized as: 1) generalized mathematical analysis for circuit simulation of coupled interconnects with frequency variant circuit parameters, 2) new simulation algorithm and software development for interconnect circuit simulation, 3) verification of the simulation algorithm and frequency variant interconnect parameter model by simulation and time domain measurements, 4) validation of the previous simplified modeling assumptions of negligible resistive and conductive coupling (see Chapter 4) and indirect inductance matrix calculation from the interconnect capacitance matrix (see Chapter 5), 5) development of equivalent circuits for pad parasitics which are required for on-chip calibration of any test device, and 6) accurate interconnect circuit-parameter prediction. All of these results can be used directly or with minor modification for high-speed VLSI circuit design, microwave circuit design, advanced packaging, and test-device characterization.

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE STUDY

The critical performance bottleneck of the next generation of state of art VLSI circuits may be due to interconnects. VLSI interconnects which play a pivotal role in high performance VLSI circuits have analyzed, measured, modeled, and simulated in this dissertation. New research results include s-parameter-measurement-based characterization methodologies, frequency variant interconnect parameter modeling, and the development of new simulation techniques verified by high speed time domain measurements.

7.1 Summary

A methodology for extracting high-frequency IC interconnect transmission parameters directly from s-parameter measurements has been demonstrated using on-chip test structures. The methodology consists of: 1) building on-chip interconnect structures for microwave test, 2) characterizing and subtracting measurement system parasitics, 3) extracting the transmission line impedance and propagation constant (attenuation constant and phase constant) from the calibrated data, and 4) extracting the Telegrapher's Equation transmission parameters (R, L, C, and G). Additional on-chip calibration permits subtraction of pad parasitic effects. This methodology is demonstrated over a 45 MHz to 20 GHz frequency range using a 1-cm long, 4-μm wide IC interconnect built in an

advanced BiCMOS process technology. Variation in interconnect impedance and capacitance indicate two signal propagation modes. Significant substrate-based loss is measured at microwave frequencies.

Multiline interconnects are mathematically modeled as a matrix form of Telegrapher's equation. The equations are completely solved. The solution vectors are represented in terms of propagation constant and characteristic impedance. These two important parameters are again represented in terms of interconnect circuit parameter matrices. Although the coupled-line parameter extraction is very complicated, an approximate interconnect parameter-extraction method is introduced. The newly developed simplified extraction method employs both single line s-parameter measurements and low frequency capacitance measurements to determine coupled line interconnect circuit parameters.

A first level metal IC interconnect model has been developed for high speed and high density VLSI circuit design based on characterization. Prior interconnect models exclude effects such as capacitive fringing, dielectric loss, and the influence of substrate conductance. In contrast, the new model considers all these effects. Moreover, this model represents fine line interconnect as well as wide line interconnect behavior over a 20 GHz frequency range. The model parameters are compared with scattering parameter measurements as well as numerical simulation based on PISCES-IIB. Excellent agreement has been shown with parameters extracted from s-parameter measurements.

Time domain signal variations have been simulated by integrating research results with new simulation techniques. Very fast signal transients, propagation, and crosstalk simulations on coupled

interconnect lines have been performed and then verified by time domain measurements, using frequency variant parameters and arbitrary loads. A generalized interconnect transfer function that can be applied to any interconnect circuit has been developed in the frequency domain. The inverse Fourier transform has been used for calculating time domain signals. S-parameter-based IC interconnect models and PISCES-IIB simulations are performed to determine the interconnect parameters. Empirical expressions and low frequency measurements are compared with the results.

Finally the generalized interconnect transfer function is used to compare conventional interconnect modeling such as constant LC, RC, and RLC to the accurate frequency variant RLCG model. Exact signal transient, propagation, and coupling noise on the on-chip interconnects can be predicted with the new frequency variant RLCG model. Time domain measurements verifications using HP54121T sampling oscilloscope show excellent agreement with simulation results.

7.2 Suggestion for Future Work

Future technology for VLSI circuits will consider device scaling and 3-dimensional interconnections. The importance of interconnects will be greatly increased as technologies advances. The literature reports multilevel interconnects not only are dominant in determining the chip size, speed performance, reliability, and yield, but also affect the profitability of all integrated circuits [Sax92]. Therefore, high frequency multiple layer interconnect characterization as well as multiline characterization for more than two lines must be developed. The layers of

metal signal paths may extend to six or more levels of interconnects in the next decade. To develop these design criteria, industry will need interconnect characterization. This characterization can be solved easily by extending the fundamental concepts of this dissertation.

Next, interconnect circuit simulations comprising active devices must be realized. In reality, the circuits are composed of active devices, interconnects, and parasitics. Therefore, all these component models must be integrated together for accurate simulations. Then, advanced high performance circuit design becomes possible.

Switching noise due to power and ground distribution should be more carefully characterized and modeled for complicated VLSI circuits and packagings. Parasitics due to packaging, i.e., lead frame inductance and reflection, must be accurately modeled.

As the interconnect lines become finer and longer, reliability related to interconnect such as electromigration, stress, contacts, and multilayer structures will become a serious problem. Thus, interconnect characterization and analysis must be performed. New material characterizations as well as models for metal alloys, polysilicon line, and diffusion line must be developed [Sax92]. High frequency characterization and analysis will become necessary for these materials.

System level performance optimization [Bak92] will become the most important issue in the future of the IC industry because today's performance improvement by device scaling will reach a limit. In other words, the VLSI circuit performance improvement in next century may not be possible by scaling but by system level optimization. System level performance modeling is an integral analysis that includes the chip-level parasitics, package-level-parasitics, on-chip interconnect analysis, signal

integrity, and power distribution. In this next century's system level performance modeling, interconnect performance modeling will play a pivotal role.

After developing all these analyses and models, the models must be implemented into the existing circuit simulation tools such as SPICE. Thereby, it will be possible to safely design the next generation of high speed ULSI circuits on CAD systems.

APPENDIX A
S-PARAMETER CALIBRATION OF TWO PORT NETWORKS

Microwave s-parameter characterization equipment has inherent error sources that must be eliminated from measurement data. This elimination processes that produces actual DUT parameters is called calibration. Thus, equipment calibration is the essential part of good s-parameter characterization of a DUT [Fit78, Hp85]. In order to subtract out the measurement errors, error model for signals must be developed and then the measured s-parameter data has to be taken to characterize error signals. This data is taken using calibration standards. Then the error model coefficients are calculated for the error models from the error data. Finally, test device data is taken and these error model is subtracted from this data.

For the one port network, error signals are due to directivity, frequency tracking, and mismatch between the DUT and the measurement system. Directivity error (E_{11}) implies that the signal that never reaches the DUT. The signal leaks off or reflects before it arrives at the DUT due to the imperfection of the signal detection device (directional coupler), the adapters and test cables that physically connects to the DUT. Frequency tracking and response errors (E_{21} and E_{12}) represent the signal loss going to and from the DUT in the test system. These parameters are the composite response of many components such as couplers, cables, and mixers. Finally, source match error (E_{22}) results from reflections due to the mismatch between a DUT and a measuring system. These signals bounce back and forth between

the DUT and measurement system. This is a major error source when the DUT impedance is poorly matched with the test system. The error models for the one port network are modeled in Fig. A-1. Notice in Fig. A-1 that E_{21} and E_{12} terms appear together as a product. Then, from the signal flow analysis, the measured reflection coefficient becomes,

$$S_{11m} = E_{11} + \frac{S_{11a}(E_{21}E_{12})}{1 - E_{22}S_{11a}} \tag{A-1}$$

The S_{11m} value is the measured s-parameter value and the S_{11a} value is the actual test device value. Since the above equation has the 3 unknowns, the 3 independent boundary conditions for the equation must be acquired and solved simultaneously. Measuring opens, shorts, and matched loads (50 ohm) with HP calibration kits or ISS (Impedance Standard Substrate which is built on wafer) three independent equations can be obtained. First, a 50 Ohm load is measured (reflection coefficient is $S_{11a} = 0$) Equation (A-1) becomes,

$$S_{11m} = E_{11}. \tag{A-2}$$

Second, the measurement of short circuit (reflection coefficient is $S_{11a} = 1\angle 180^{\circ}$) provides,

$$S_{11m} = E_{11} + \frac{(-1)(E_{21}E_{12})}{1 - E_{22}(-1)}. \tag{A-3}$$

Finally, measuring the reflection coefficient of an open circuit ($S_{11a} = 1\angle\theta^{\circ}$) yields,

$$S_{11m} = E_{11} + \frac{(1)(E_{21}E_{12})}{1 - E_{22}(1)} = E_{11} + \frac{(E_{21}E_{12})}{1 - E_{22}}. \tag{A-4}$$

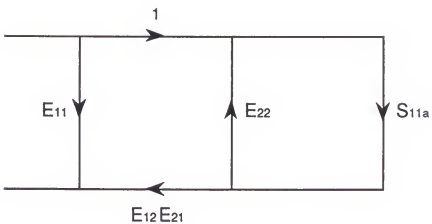


Fig. A-1 One port network error model.

Thus, solving above three equations simultaneously, the reflection error model values (E_{11}, E_{12}, E_{21}, and E_{22}) are determined. These error model values are plugged into original error model equation so that the actual DUT reflection coefficient S_{11a} is found.

In order to perform transmission calibrations for tracking, leakage, and load mismatchs for two port characterization a more complicated error model has to be developed. The complete error model for two port characterization which includes 12 error terms is shown in Fig. A-2. By solving the error models with signal flow graph analysis the forward transmission signal S_{21} is,

$$S_{21a} = \frac{\left(\frac{S_{21m} - E_{xf}}{E_{tf}}\right)\left[1 + \left(\frac{S_{22m} - E_{df}}{E_{rr}}\right)(E_{sr} - E_{lf})\right]}{\left[\left(1+\frac{(S_{11m} - E_{df})}{E_{rf}}\right)E_{sf}\right]\left[\left(1+\frac{(S_{22m} - E_{df})}{E_{rr}}\right)E_{sr}\right] - \left(\frac{S_{21m} - E_{xf}}{E_{tf}}\right)\left(\frac{S_{12m} - E_{xr}}{E_{tr}}\right)E_{lr}\,E_{lf}} . \tag{A-5}$$

Applying graph theory to Fig.A-2, the equation (A-5) and other actual scattering parameters (S_{11}, S_{12}, and S_{22}) are derived. The waves entering at port-1 are,

$$a_1 = 1 + E_{sf}b_1,$$

$$a_2 = E_{lf}b_2. \tag{A-6}$$

The measured s-parameters at port-1 are

$$S_{11m} = E_{df} + E_{rf}b_1,$$

$$S_{21m} = E_{xf} + E_{tf}b_2. \tag{A-7}$$

The scattered waves at each port under a forward direction are

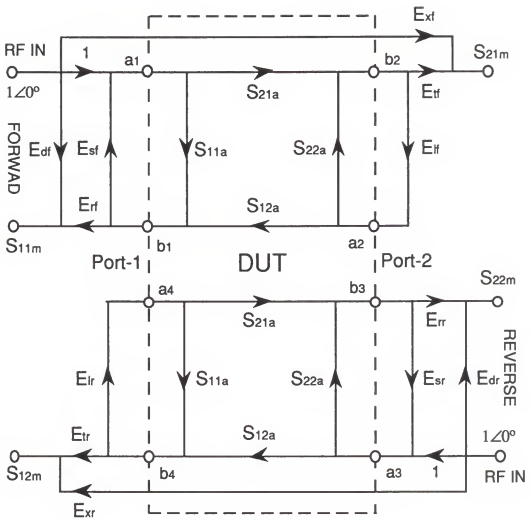


Fig. A-2 Two port s-parameter network error model.

$$b_2 = S_{21a}a_1 + S_{22a}a_2 = \frac{S_{21m} - E_{xf}}{E_{tf}},$$

$$b_1 = S_{12a}a_2 + S_{11a}a_1 = \frac{S_{11m} - E_{df}}{E_{rf}}. \tag{A-8}$$

Thus, combining the above equations, the entering waves in the forward direction are rewritten as

$$a_1 = 1 + E_{sf}\frac{S_{11m} - E_{df}}{E_{rf}},$$

$$a_2 = E_{tf}\frac{S_{21m} - E_{xf}}{E_{tf}}. \tag{A-9}$$

Similarly, entering waves under a reverse direction are

$$a_3 = 1 + E_{sr}b_3,$$

$$a_4 = E_{tr}b_4. \tag{A-10}$$

The measured scattering parameters at the port-2 are

$$S_{22m} = E_{dr} + E_{rr}b_3,$$

$$S_{12m} = E_{xr} + E_{tr}b_4. \tag{A-11}$$

The scattered waves at each port under the reverse direction are

$$b_4 = S_{12a}a_3 + S_{11a}a_4 = \frac{S_{12m} - E_{xr}}{E_{tr}},$$

$$b_3 = S_{21a}a_4 + S_{22a}a_3 = \frac{S_{22m} - E_{dr}}{E_{rr}}. \tag{A-12}$$

Thus, plugging (A-11) and (A-12) into (A-10), the entering waves at port-2 are rewritten as

$$a_3 = 1 + E_{sr}\frac{S_{22m} - E_{dr}}{E_{rr}},$$

$$a_4 = E_{lr}\frac{S_{12m} - E_{xr}}{E_{tr}}. \tag{A-13}$$

In order to simplify the expression the followings are defined,

$$A = \frac{S_{11m} - E_{df}}{E_{rf}} = b_1,$$

$$B = \frac{S_{21m} - E_{xf}}{E_{tf}} = b_2,$$

$$C = \frac{S_{12m} - E_{xr}}{E_{tr}} = b_4,$$

$$D = \frac{S_{22m} - E_{dr}}{E_{rr}} = b_3. \tag{A-14}$$

Then the scattering waves can be rewritten as

$$a_1 = 1 + E_{sf}A,$$

$$a_2 = E_{lf}B,$$

$$a_3 = 1 + E_{sr}D,$$

$$a_4 = E_{lr}C. \tag{A-15}$$

Since the scattered waves at port-1 are

$$b_1 = S_{11a}a_1 + S_{12a}a_2,$$

$$b_4 = S_{11a}a_4 + S_{12a}a_3, \tag{A-16-a}$$

the true DUT scattering parameters at port-1 are as follows

$$S_{11a} = \frac{b_1 a_3 - a_2 b_4}{a_1 a_3 - a_2 a_4} = \frac{(1 + D\,E_{sr})A - E_{lf}B\,C}{[(1 + A)E_{sf}][(1 + D)E_{sr}] - C\,B\,E_{lr}E_{lf}},$$

$$S_{12a} = \frac{a_1 b_4 - b_1 a_4}{a_1 a_3 - a_2 a_4} = \frac{C[1 + A\,(E_{sf} - E_{lr})]}{[(1 + A)E_{sf}][(1 + D)E_{sr}] - C\,B\,E_{lr}E_{lf}}. \tag{A-17-a}$$

Likewise, the scattered waves at port-2 are

$$b_2 = S_{21a}a_1 + S_{22a}a_2,$$

$$b_3 = S_{21a}a_4 + S_{22a}a_3, \qquad \text{(A-16-b)}$$

the true DUT scattering parameters at port-2 are as follows

$$S_{21a} = \frac{b_2 a_3 - a_2 b_3}{a_1 a_3 - a_2 a_4} = \frac{B[1 + D(E_{sr} - E_{lf})]}{[(1 + A)E_{sf}][(1 + D)E_{sr}] - C\,B\,E_{lr}E_{lf}},$$

$$S_{22a} = \frac{a_1 b_3 - b_2 a_4}{a_1 a_3 - a_2 a_4} = \frac{(1 + A\,E_{sf})D - E_{lr}BC}{[(1 + A)E_{sf}][(1 + D)E_{sr}] - C\,B\,E_{lr}E_{lf}}. \qquad \text{(A-17-b)}$$

Q.E.D

These true DUT scattering parameter, (A-16) and (A-17) are automatically determined in the Automatic Network Analyzer (ANA) such as HP8510 by using standard calibration techniques. The standard calibration algorithm is shown on Fig. A-3.

Algorithm: Full Two Port Calibration

input: known device measurement data

output: actually calibrated DUT_S-parameter data

PROCEDURE CALIBRATION (input, output) // two port network cal.

begin

set **ISS map**

for i = 1 to 2 // i is the port number

measure **load**; // 50 ohm

measure **short**;

measure **open**;

reverse DUT physically;

end_for

set **THRU** device;

for i = 1 to 2 // i is the port number

measure S_{1i} ;

measure S_{2i} ;

reverse DUT physically;

end_for

compute **true DUT_S-parameters**

end_begin

Fig. A-3 Full two port network calibration algorithm.

APPENDIX B
LOW FREQUENCY CAPACITANCE MEASUREMENTS

In low frequency signal transmission on the IC, capacitance and resistance play a pivotal role in interconnect circuit performance. Resistance can be easily calculated in this frequency range but the capacitance is not readily calculated. However, knowing capacitance is vital to determine the circuit delay and crosstalk noise (coupling noise) on an IC chip. This is determined by the capacitance of all wring nets. Using a simple parallel plate capacitance computation is not sufficiently accurate in modern ICs. Thus, low frequency capacitance measurement techniques for on-chip interconnect are described in detail in this Appendix.

Basic theoretical concepts such as physical definition of capacitance and difference between conventional SPICE-like capacitance definition and short circuit capacitance definition are described. This is followed by a discussion of two terminal capacitance concepts. These various definitions of capacitance are related with simple forms of expressions which can be easily extracted from low frequency C-V measurements.

B.1 Definition of Capacitance

A physically rigorous definition of capacitance is presented here. For a multiconductor transmission line, the potentials (p-matrix) are given by

$$\begin{aligned}
\phi_1 &= p_{11}Q_1 + p_{12}Q_2 + \cdots + p_{1n}Q_n \\
\phi_2 &= p_{21}Q_1 + p_{22}Q_2 + \cdots + p_{2n}Q_n \\
&\vdots \\
\phi_n &= p_{n1}Q_1 + p_{n2}Q_2 + \cdots + p_{nn}Q_n
\end{aligned} \tag{B-1}$$

where

$\phi_i \equiv$ potential at conductor i ,

$Q_i \equiv$ charge at conductor i ,

$p_{ij} \equiv$ coefficient of potential between conductor i and j.

In order to understand the concepts, the following two conductor example is defined. Conductor 1 is signal line and conductor 2 is a ground,

$$\begin{aligned}
\phi_1 &= p_{11}Q_1 + p_{12}Q_2 \\
\phi_2 &= p_{21}Q_1 + p_{22}Q_2 .
\end{aligned} \tag{B-2}$$

Then, since $Q_1 = Q$ and $Q_2 = -Q$,

$$\phi_1 - \phi_2 = (p_{11} + p_{22} - p_{12} - p_{21})Q . \tag{B-3}$$

Thus,

$$C \equiv \frac{Q}{\phi_1 - \phi_2} \equiv \frac{Q}{V} = \frac{1}{(p_{11} + p_{22} - p_{12} - p_{21})}. \tag{B-4}$$

From this, we can know that capacitance is represented as coefficients of potential. Note, that p_{ij} is a purely geometrical parameter. This definition shows rigorous concepts about capacitance, however, the discussion seems to complex to use for multiconductor interconnect systems or engineering applications. Fortunately, formulas are related to the short circuit capacitance matrix which can be easily calculated or measured. It is shown that the P-matrix is equal to the inverse matrix of the short circuit

capacitance [Ram65][Rue75]. In order to produce relationship between measurable (short circuit capacitance) parameters and (B-1) is restated as,

$$[\phi] = [P][Q], \tag{B-5}$$

Thus,

$$[Q] = [P]^{-1}[\phi] \equiv [X][\phi] \tag{B-6}$$

Since the $[\phi]$ has the dimensions of voltage and the unit of $[Q]$ is Coulomb, the $[P]^{-1}$ in (B-6) has the dimension of capacitance. Therefore,

$$[X] \equiv [P]^{-1} \tag{B-7}$$

the charge equations of the multiconductor systems become

$$\begin{aligned} Q_1 &= x_{11}\phi_1 + x_{12}\phi_2 + \cdots + x_{1n}\phi_n \\ Q_2 &= x_{21}\phi_1 + x_{22}\phi_2 + \cdots + x_{2n}\phi_n \\ &\vdots \\ Q_n &= x_{n1}\phi_1 + x_{n2}\phi_2 + \cdots + x_{nn}\phi_n. \end{aligned} \tag{B-8}$$

Then, what does x_{ij} mean ? In order to understand the physical meaning, think of a system of 3 signal conductors and one reference conductor. The charge equations with the node capacitances can be established as

$$\begin{aligned} Q_1 &= C_{11}\phi_1 + C_{12}(\phi_1 - \phi_2) + C_{13}(\phi_1 - \phi_3) \\ &= (C_{11} + C_{12} + C_{13})\phi_1 + (-C_{12})\phi_2 + (-C_{13})\phi_3 \\ Q_2 &= C_{21}(\phi_2 - \phi_1) + C_{22}\phi_2 + C_{23}(\phi_2 - \phi_3) \\ &= (-C_{21})\phi_1 + (C_{21} + C_{22} + C_{23})\phi_2 + (-C_{31})\phi_3 \\ Q_3 &= C_{31}(\phi_3 - \phi_1) + C_{32}(\phi_3 - \phi_2) + C_{33}\phi_3 \\ &= (-C_{31})\phi_1 + (-C_{32})\phi_2 + (C_{31} + C_{32} + C_{33})\phi_3. \end{aligned} \tag{B-9}$$

Comparing the coefficients of the (B-6) and (B-9),

$$X_{ii} = \sum_{i=1}^{n} C_{ij}, \tag{B-10}$$

$$X_{ij} = - C_{ij}. \tag{B-11}$$

The equation (B-10) and (B-11) are exactly equal to the definition of short circuit capacitance. Thus,

$$[X] = [C]_s. \tag{B-12}$$

B.2 Short Circuit Capacitance and Measurements

In the previous section, the capacitive induction coefficients, conventional capacitance, and short circuit capacitance are defined and their relationships have been derived. Among them the only measurable definition of capacitance is short circuit capacitance (particularly in multiconductor systems) even if the others are conceptionally physical and easy to understand. In this section, conventional capacitance and short circuit capacitance are related to each other by somewhat different method than the previous section. Then, a new conception of two terminal capacitance which is measurable quantity is presented. Finally, short circuit capacitance is represented in terms of the two terminal capacitance.

Now let us start with the introduction of the self capacitance and mutual capacitance. In n conductor systems the charge per unit length on the i-th conductor, Q_i, is given from (B-9) by

$$Q_i = C_{ii}V_i + \sum_{j=1,\, j\neq i}^{n} C_{ij}(V_i - V_j) \tag{B-13}$$

where

$V_i \equiv$ voltage of the i-th conductor with reference to GND

$C_{ii} \equiv$ capacitance between i-th conductor and GND

$C_{ij} \equiv$ coupling capacitance between i-th conductor and j-th conductor.

Note, the above C_{ii} and C_{ij} are definitions for a SPICE like simulation program. However, for the theoretical analysis, (B-13) can be rewritten in terms of a short circuit matrix. The short circuit capacitance matrix which is analogous to the node admittance matrix and finds frequent applications is defined as [Rue75],

$$[C_s] \equiv \begin{bmatrix} C_{s11} & \cdots & C_{s1n} \\ \vdots & \ddots & \vdots \\ C_{sn1} & \cdots & C_{snn} \end{bmatrix} \tag{B-14}$$

where for $j = i$,

$$C_{sji} = C_{sii} \equiv \sum_{j=1}^{n} C_{ij} \tag{B-15}$$

and for $j \neq i$,

$$C_{sij} \equiv -C_{ij}. \tag{B-16}$$

Thus (B-13) is rewritten,

$$\begin{aligned} Q_i &= C_{ii}V_i + \sum_{j=1,\ j\neq i}^{n} C_{ij}V_i - \sum_{j=1,\ j\neq i}^{n} C_{ij}V_j \\ &= \left(C_{ii} + \sum_{j=1,\ j\neq i}^{n} C_{ij}\right)V_i - \sum_{j=1,\ j\neq i}^{n} C_{ij}V_j \\ &= \sum_{j=1}^{n} C_{ij}V_i - \sum_{j=1,\ j\neq i}^{n} C_{ij}V_j \end{aligned} . \tag{B-17}$$

Hence from (B-7), (B-8), and (B-9),

$$Q_i = \sum_{j=1}^{n} C_{sij} V_j \tag{B-18}$$

where

C_{sij} ≡ short circuit capacitance.

The main reason why capacitance is defined as short circuit capacitance matrix is that it is easier to obtain short circuit capacitances either from the experimental measurements or from the numerical computations. Thus, the relationship between the conventional capacitance definition, C_{ij} and the short circuit capacitance definition, C_{sij} , of (B-15) and (B-8) is,

$$C_{ij} = - C_{sij} \quad j \neq i \ . \tag{B-19}$$

$$C_{sii} = \sum_{j=1}^{n} C_{ij} \tag{B-20-1}$$

that is,

$$C_{ii} = \sum_{j=1}^{n} C_{sij} \ . \tag{B-20-b}$$

Now, defining "A" as an active set, nodes are assigned to active set or inactive set by following criteria [Wee70],

$$V_i = V \quad if \ i \in A$$

$$V_i = 0 \quad if \ i \notin A \ , \tag{B-21}$$

the two terminal capacitance per unit length (easily measured) is defined as the capacitance between these two subsets. In other words, the capacitance between all node set $x \in A$ (active node set) and all node set $y \notin A$ (inactive node set),

$$C_{2T}^{A} = \sum_{i \in A} \frac{Q_i}{V} \ . \tag{B-22}$$

Then, the short circuit capacitance can be represented in terms of the two terminal capacitance,

$$C_{sii} = C_{2T}^{i} \tag{B-23-a}$$

$$C_{sij,\ i \neq j} = \frac{1}{2}\left(C_{2T}^{\{i,j\}} - C_{2T}^{\{i\}} - C_{2T}^{\{j\}}\right) \tag{B-23-b}$$

(*Proof*)

Since from (B-18) and (B-22)

$$Q_i = \sum_{j=1}^{n} C_{sij} V_j$$

and

$$C_{2T}^{A} = \sum_{i \in A} \frac{Q_i}{V},$$

the two terminal capacitance with conductor i and conductor j active is

$$C_{2T}^{\{i,j\}} = \sum_{k=i,j} \frac{Q_k}{V} = \frac{Q_i}{V} + \frac{Q_j}{V}. \tag{B-24}$$

Since the active conductors are i-th conductor and j-th conductor,

$V_i = V_j = V$ *and* $V_k = 0$ *where* $k = 1, 2, 3, \cdots, n\ ;k \neq i,\ k \neq j$.

Thus,

$$Q_i = C_{sii} V_i + C_{sij} V_j$$

$$Q_j = C_{sjj} V_j + C_{sji} V_i. \tag{B-25}$$

Plugging (B-24) into (B-25),

$$C_{2T}^{\{i,j\}} = C_{sii} + C_{sij} + C_{sjj} + C_{sji}. \tag{B-26}$$

Since

$$C_{sij} = C_{sji}, \quad C_{sii} = C^{i}_{2T}, \quad \text{and} \quad C_{sjj} = C^{j}_{2T},$$

the two terminal capacitance become

$$C^{\{i,j\}}_{2T} = 2C_{sij} + C^{i}_{2T} + C^{j}_{2T}. \tag{B-27}$$

Hence, finally it become

$$C_{sij} = \frac{1}{2}\left(C^{\{i,j\}}_{2T} - C^{i}_{2T} - C^{j}_{2T} \right). \tag{B-28}$$

Q. E. D.

B.3 Relationship of Various Definitions

It is sometimes very confusing to distinguish the definition between the conventional capacitance and the short circuit capacitance definition in various systems. The question, "is the single line capacitance the short circuit capacitance or the conventional capacitance ?" frequently happens. Both values are the same for the single line. Then, are the self-capacitances of symmetrical double conductors equal to the single isolated conductor self-capacitance ? The answer is no !! Thus, the capacitance matrix of the coupled interconnect lines can be expressed,

$$[C] = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix}_{conventional} \tag{B-29}$$

$$= \begin{bmatrix} C_{s11} + C_{s12} & -C_{s12} \\ -C_{s21} & C_{s22} + C_{s21} \end{bmatrix}_{short\ circuit} \tag{B-30}$$

$$\neq \begin{bmatrix} C_{single\text{-}line} + C_{s12} & -C_{s12} \\ -C_{s21} & C_{single\text{-}line} + C_{s21} \end{bmatrix}_{extraction}. \tag{B-31}$$

In fact, the isolated capacitance ($C_{single\text{-}line}$) is equal to "C_{11} + (C_{12} // C_{22}) " of a two conductors system. Then

$$C_{single\text{-}line} = C_{11} + \frac{C_{12}C_{22}}{C_{12} + C_{22}}$$

$$= C_{11} + \frac{C_{12}C_{11}}{C_{12} + C_{11}}. \tag{B-32}$$

If it is rewritten in terms of C_{11},

$$C_{11} = \frac{C_{single\text{-}line} - 2C_{12} + \sqrt{C_{single\text{-}line}^2 + 4C_{12}^2}}{2}. \tag{B-33}$$

Thus, its asymptote value is,

$$C_{11} = \begin{cases} C_{single\text{-}line} & for \quad C_{single\text{-}line} >> C_{12} \\ \dfrac{C_{single\text{-}line}}{2} & for \quad C_{single\text{-}line} << C_{12} \end{cases}. \tag{B-34}$$

Another thing that must be considered is the physical meaning of two terminal capacitance measurements. The two terminal capacitance in which conductor 1 and conductor 2 are shorted becomes,

$$C_{2T}^{\{1,2\}} = 2C_{11} = 2C_{22}. \tag{B-35}$$

The two terminal capacitance in which the conductor 2 and a reference node are shorted, i.e.,

$$C_{2T}^{\{1\}} = C_{11} + C_{12} = C_{2T}^{\{2\}}. \tag{B-36}$$

Thus, the coupling capacitance become

$$C_{2T}^{\{1\}} - \frac{C_{2T}^{\{1,2\}}}{2} = C_{12}. \tag{B-37}$$

Note here that (B-37) is exactly equal to (B-28) for symmetric systems. Furthermore, short circuit self-capacitance is in general frequency

dependent at high frequency. In order to simulate the interconnect circuits, a single line model which is frequency variant model must be used and coupling capacitance can be obtained from other methods such as PISCES-II simulation or analytical expressions.

B.4 Calibration Method (De-embedding)

The real capacitance measurement of a pattern on wafer require pad calibration which is called de-embedding. Simple de-embedding techniques for two terminal capacitance measurements are presented here.

Open structure measurements: without any connection between the probe tip and test structure, the capacitance is measured and then it is saved as a value "Z". This is used for the measurement apparatus correction.

Measurement of open structure: the one side pad is measured. It is used for the opposite side pad calibration. The measured data is saved as value "A".

DUT measurements: DUT is measured and then saved as value "B". Then, the true DUT capacitance can be calculated as

$$C = B - A - (A - Z). \tag{B-38}$$

The above expression must hold throughout the experiments for any capacitance such as single line capacitance or multiline short circuit capacitance measurements.

APPENDIX C
CIRCUIT RESPONSE OF MULTILINE INTERCONNECTS

Interconnect circuits composed of multiconductors are modeled by a matrix form of Telegrapher's equations. Solving the matrix equations is divided into two processes, i.e., obtaining eigenvalues by solving the eigenvalues equations and then obtaining solution vectors (eigenvectors) corresponding to the eigenvalues. Once the solution vectors are found, interconnect circuit response can be determined from the superposition theorem. Therefore, first the eigenvalue equations of the matrix equation must be solved. For the m-th eigenmode, eigenvalue equation is

$$\left\{\gamma_m^2[U] - [Z_s][Y_p]\right\}[V_m(0)] = 0 \,. \tag{C-1}$$

A set of n column vectors { $[V_1(0)]$, $[V_2(0)]$, $\cdots$ $[V_n(0)]$ } are called as the eigenvectors and γ_m^2 as the m-th eigenvalue of the system $[Z_s][Y_p]$. Since an n conductor system has n eigenmodes, let the set of eigenvectors be $[S_v]$ which is $n \times n$ matrix and is called voltage eigenmatrix. That is,

$$[S_v] \triangleq \left[\, [V_1(0)], [V_2(0)], [V_3(0)], \cdots, [V_n(0)] \,\right]. \tag{C-2}$$

Representing m-th mode eigenvector as component eigenvector of eigenmatrix,

$$[S_m] \triangleq [V_m(0)] \qquad \text{for } m = 1, 2, \cdots, n \,, \tag{C-3}$$

the voltage eigenmatrix can be represented by

$$[S_v] = \left[\, [S_1],\ [S_2],\ \cdots,\ [S_n] \,\right] \tag{C-4}$$

where $[S_v]$ is the n x n matrix and $[S_m]$ is the column vector. Thus,

γ_1^2 —corresponding eigenvector→ $[S_1]$ *column vector*

γ_2^2 —corresponding eigenvector→ $[S_2]$ *column vector*

$\vdots$

γ_n^2 —corresponding eigenvector→ $[S_n]$ *column vector*.

Hence, from the superposition theorem, the solution $V(x)$ is,

$$\begin{aligned} V(x) \;=\; & c_1 exp(-\gamma_1 x)[S_1] + d_1 exp(+\gamma_1 x)[S_1] \\ & + c_2 exp(-\gamma_2 x)[S_2] + d_2 exp(+\gamma_2 x)[S_2] \\ & \qquad \vdots \\ & + c_i exp(-\gamma_i x)[S_i] + d_i exp(+\gamma_i x)[S_i] \\ & \qquad \vdots \\ & + c_n exp(-\gamma_n x)[S_n] + d_n exp(+\gamma_n x)[S_n]. \end{aligned} \tag{C-5}$$

Rewriting (C-5) as the matrix form,

$$\begin{aligned} [V(x)] = & \left[\, [S_1][S_2]\cdots[S_n] \,\right] \begin{bmatrix} e^{-\gamma_1 x} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & e^{-\gamma_n x} \end{bmatrix} \begin{bmatrix} c_1 \\ \vdots \\ c_n \end{bmatrix} \\ & + \left[\, [S_1][S_2]\cdots[S_n] \,\right] \begin{bmatrix} e^{\gamma_1 x} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & e^{\gamma_n x} \end{bmatrix} \begin{bmatrix} d_1 \\ \vdots \\ d_n \end{bmatrix}, \end{aligned} \tag{C-6}$$

Expression (C-6) can be again rearranged by

$$[V(x)] = [S_v][E(x)][C_1] + [S_v][E(x)]^{-1}[C_2] \tag{C-7}$$

where $[E(x)]$ is the diagonal matrix of

$$[E(x)] \triangleq \begin{bmatrix} e^{-\gamma_1 x} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & e^{-\gamma_n x} \end{bmatrix}$$

and $[C_1]$ and $[C_2]$ are constant column vectors of

$$[C_1] = \begin{bmatrix} c_1 \\ \vdots \\ c_n \end{bmatrix} \qquad \textit{and} \qquad [C_2] = \begin{bmatrix} d_1 \\ \vdots \\ d_n \end{bmatrix}.$$

From the above $[V(x)]$, we can obtain the current equations plugging (C-7) into (4-1) in Chapter 4,

$$[I(x)] = [S_i][E(x)][C_1] - [S_i][E(x)]^{-1}[C_2] \qquad \text{(C-8-a)}$$

$$\textit{where} \quad [S_i] = [Z_s]^{-1}[S_v]\,[\Lambda]. \qquad \text{(C-8-b)}$$

Assigning

$$[\Lambda] = diag\{\gamma_1, \gamma_2, \cdots, \gamma_n\}, \qquad \text{(C-9)}$$

$$\frac{d[E(x)]}{dx} = [\Lambda][E(x)].$$

From equation (C-7) and (C-8),

$$[V(x)] = [S_v][E(x)][C_1] + [S_v][E(x)]^{-1}[C_2] \qquad \text{(C-10)}$$

$$[I(x)] = [S_i][E(x)][C_1] - [S_i][E(x)]^{-1}[C_2]. \qquad \text{(C-11)}$$

Thus, the boundary condition for the current at x = 0 becomes

$$[I(0)] = [S_i][C_1] - [S_i][C_2]$$

$$= [\,[S_i]\,[-S_i]\,]\begin{bmatrix} C_1 \\ C_2 \end{bmatrix}. \qquad \text{(C-12)}$$

Also, by rearranging (C-12)

$$[C_1] - [C_2] = [S_i]^{-1} [I(0)] . \tag{C-13}$$

Similarly, from the voltage boundary condition

$$\begin{aligned} [V(0)] &= [S_v][C_1] + [S_v][C_2] \\ &= \begin{bmatrix} [S_v] & [-S_v] \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} . \end{aligned} \tag{C-14}$$

Ultimately (C-14) becomes

$$[C_1] + [C_2] = [S_v]^{-1} [V(0)] . \tag{C-15}$$

From the boundary condition for current and voltage at x = D,

$$[I(D)] = [S_i][E(D)][C_1] - [S_i][E(D)]^{-1} [C_2] \tag{C-16}$$

$$[V(D)] = [S_v][E(D)][C_1] + [S_v][E(D)]^{-1} [C_2] . \tag{C-17}$$

Therefore,

$$\begin{bmatrix} [I(0)] \\ [I(D)] \end{bmatrix} = \begin{bmatrix} [S_i] & -[S_i] \\ [S_i][E(D)] & -[S_i][E(D)]^{-1} \end{bmatrix} \begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix} \tag{C-18}$$

$$\begin{bmatrix} [V(0)] \\ [V(D)] \end{bmatrix} = \begin{bmatrix} [S_v] & [S_v] \\ [S_v][E(D)] & [S_v][E(D)]^{-1} \end{bmatrix} \begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix} . \tag{C-19}$$

Inverting (C-19),

$$\begin{bmatrix} [C_1] \\ [C_2] \end{bmatrix} = \begin{bmatrix} [S_v] & [S_v] \\ [S_v][E(D)] & [S_v][E(D)]^{-1} \end{bmatrix}^{-1} \begin{bmatrix} [V(0)] \\ [V(D)] \end{bmatrix} . \tag{C-20}$$

Plugging (C-20) into (C-18),

$$\begin{bmatrix} [I(0)] \\ [I(D)] \end{bmatrix} = \begin{bmatrix} [S_i] & -[S_i] \\ [S_i][E(D)] & -[S_i][E(D)]^{-1} \end{bmatrix} \begin{bmatrix} [S_v] & [S_v] \\ [S_v][E(D)] & [S_v][E(D)]^{-1} \end{bmatrix}^{-1} \begin{bmatrix} [V(0)] \\ [V(D)] \end{bmatrix}. \tag{C-21}$$

APPENDIX D
SKIN EFFECT IN FINE LINE INTERCONNECTS

D.1 Skin Effect for a Moderately-Wide Conductor

The sheet resistance for an infinitely thick conductor is,

$$R_s = \frac{\rho}{\delta} \; Ohms/Square \qquad \text{(D-1)}$$

Here, δ is the skin depth for an infinitely thick conductor. This conductor has an exponentially decreasing current density with depth. The effective skin depth under a finite conductor depth is modeled by Fig. D-1. Fig. D-1 shows that the skin depth, δ of a wide conducting plane of infinite thickness is defined so that the conducting area of the rectangular with points 1, 2, 3 and 4 is equal to that of the conducting area underneath the exponential curve 2 to 5. A conductor of finite thickness t has a reduced skin depth of δ_x since the current between t and 5 is not present. Thus, a modified skin depth δ_x is defined by

$$\begin{aligned} I_{total} &= \int_0^t j(0) exp\left(-\frac{x}{\delta}\right) dx \\ &= j(0)\delta\left\{1 - exp\left(-\frac{t}{\delta}\right)\right\} \\ &\triangleq j(0)\delta_x. \end{aligned} \qquad \text{(D-2)}$$

Therefore,

$$\delta_x \triangleq \delta\left\{1 - exp\left(-\frac{t}{\delta}\right)\right\}. \qquad \text{(D-3)}$$

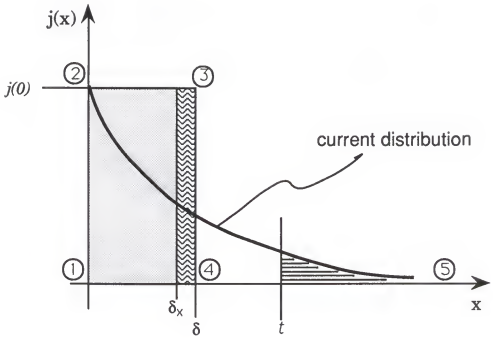


Fig. D-1 Conductor current distribution and skin depth.

D.2 Estimation of Two Dimensional Skin Depth in Microstrip

In a narrow rectangular transmission line structure the skin effect current will be on the conductor sides with field lines extending to the ground plane. For the IC interconnect (microstrip) case, field lines will extend from the substrate below the conductor to the side of a conductor. An empirical approximation for the addition current is supplied by the following,

$$\delta_y = \delta_x \frac{t}{w} \tag{D-4}$$

This can be conceptually justified because t/w is the ratio of the conductor vertical periphery to that of the horizontal periphery. Our experiments verify the side wall conduction adds additional current in this ratio. Thus, the total skin depth for a conductor of finite thickness as well as finite width is

$$\begin{aligned} \delta^* &= \delta_x + \delta_y \\ &= \delta_x \left(1 + \frac{t}{w}\right) \\ &= \delta\left(1 - exp\left(-\frac{t}{\delta}\right)\right)\left(1 + \frac{t}{w}\right) \end{aligned} \tag{D-5}$$

$$where \quad \delta = \frac{1}{\sqrt{\pi f \mu \sigma}}.$$

APPENDIX E
ALGORITHM OF SPAIL

The algorithms are composed of three parts. The first one is the user interface, SPAIL, which is coded in c-shell commands. Its function is to perform preprocessing of user input and calling extraction algorithms in subsequent parts. The second part, LINE, performs the interconnect parameter extraction without pad parasitics. Finally, algorithm DLINE extracts de-embedded line parameters.

E.1 Algorithm: User Interface

Interactive user interface shell program

Input: characters typed by user

Output: interconnect line parameters

PROCEDURE SPAIL(input, output)

request user input;

if (there is no error) then

{

if (de-embedding requested) then

{

read keyboard-based information;

make temporary files;

determine the number of data points;

do **PROCEDURE LINE**

```
                    do PROCEDURE DLINE
                }
        else
                {
                read key board-based information;
                make temporary files;
                determine the number of data points;
                    do PROCEDURE LINE
                }
        endif
}
else
        show error message;
endif

remove temporary files;
stop
end
```

E.2 Algorithm: Line

Line parameter extraction without pad parasitic calibration.

Input: S-parameter data

Output: Uncalibrated interconnect line parameter

```
PROCEDURE LINE(input, output)
    set constants;
    print head line;
    open temporary files;
    if (data format = 'r') then              // real/imaginary
        read input data in real/imaginary form;
    else                                     // mag/phase
        read input data in magnitude/phase form;
    endif
    calculate propagation constant;
        do PROCEDURE RADIAN(measured phase, real phase)
            // RADIAN is the subprocedure for calculating
            // the real phase from the measured
            // cyclical phase !!
    calculate characteristic impedance;
        do PROCEDURE RADIAN(measured phase, real phase)
    calculate line parameters;
    print output;
    stop
    end
```

E.3 Algorithm: Dline

Line parameter extraction after subtracting pad parasitics.

Input: S-parameter data files (device and open-pads)

Output: De-embedded line parameters

PROCEDURE DLINE(input, output)

```
set constants;
print head line;
open temporary files;
if (data format = 'r') then                    // real/imaginary
        read input data in real/imaginary form;
else                                           // mag/phase
        read input data in magnitude/phase form;
endif

convert S-parameter files into Y-parameters;
subtract pad parasitics Y-parameters;
convert new Y-parameters into S-parameters;
        do PROCEDURE LINE
print uncalibrated output
calculate propagation constant;
        do PROCEDURE RADIAN(measured phase, real phase)
calculate characteristic impedance;
        do PROCEDURE RADIAN(measured phase, real phase)
calculate line parameters;
print calibrated output;
```

do **PROCEDURE ZGCAL** (line parameter, new propagation
constant, and new characteristic impedance);
// **ZGCAL** calculates the propagation constant and the
// characteristic impedance after subtraction of pad
// parasitics.
print the calibrated gamma and impedance;
stop
end

REFERENCES

Agr79a A. K. Agrawal, K. M. Lee, H. M. Fowles, and L. D. Scott, "Experimental Characterization of Multiconductor Transmission Lines in the Frequency Domain," IEEE Trans. Electromagnetic Compatibility, vol. EMC-21, No.1, pp. 20-27, Feb., 1979.

Agr79b A. K. Agrawal, Howard M. Fowles, and Larry D. Scott, "Experimental Characterization of Multiconductor Transmission Lines in Inhomogeneous Media Using Time-Domain Techniques," IEEE Trans. Electromagnetic Compatibility, vol. EMC-21, No.1, pp. 28-32, Feb., 1979.

Ant83 Robert J. Antinone and Gerald W. Brown, "The Modeling of Resistive Interconnects for Integrated Circuits," IEEE Journal of Solid-State Circuits, vol. SC-18, pp. 200-203, Apr., 1983.

Bog91 Eric Bogatin and Giga Test Labs, Microwave Basic's Short Course, CA, 1992.

Bak85 H. B. Bakoglu and J. D. Meindl, "Optimal Interconnect Circuits for VLSI," IEEE Trans. Electron Devices, vol. ED-32, No.5, pp. 903-909, May., 1985.

Bak92 H. B. Bakoglu, "Interconnect for the '90s: System Level Electrical Issues," IEDM 1992 Short Course: Interconnect for the '90s, San Jose, CA, 1992.

Car69 Vincent L. Carry, Terrence R. Scott, and William T. Weeks, "Characterization of Multiple Transmission Lines Using Time Domain Reflectometry," IEEE Trans. Instruments and Measurement, vol. IM-18, No.3, pp. 166-171, Sep., 1969.

Che92 J-H. Chern, J. Huang, L. Arledge, P-C. Li, P. Yang, "Multilevel Metal Capacitance Model for CAD Design Synthesis Systems," IEEE EDL, vol.13, No.1, pp. 32-34, Jan., 1992.

Cho91 H. Cho, and D. E. Burk, "A Three Step Method for the De-embedding of High Frequency S-Parameter

Measurements," IEEE Trans. ED., vol.38, pp. 1371-1375, Jun., 1991.

Col66 Robert E. Collin, Foundations for Microwave Engineering, McGraw-Hill Inc., New York, 1966.

Com90 SuperCompact, Compact Software Inc., Los Altos, CA, 1990.

Cur85 Hermann Curtins and Arvind V. Shah, "Pulse Behavior of Transmission Lines with Dielectric Losses," IEEE Trans. CAS., vol. CAS-32, No. 8, pp. 819-826, Aug., 1985.

Deu90 A. Deutsch, G. V. Kopcsay, V. A. Ranieri, J. K. Cataldo, E. A. Galligan, W. S. Graham, R. P. McGouey, S. L. Nunes, J. R. Paraszczak, J. J. Ritsko, R. J. Serino, D. Y. Shih, and J. S. Wilczynsik, "High-Speed Signal Propagation on Lossy Transmission Lines," IBM J. Res. Develop., vol. 34, No.4, pp. 601-615, Jul., 1990.

Djo86 A. R. Djordjevic, T. K. Sakar, and R. F. Harrington, "Analysis of Lossy Transmission Lines with Arbitrary Nonlinear Terminal Networks," IEEE Trans. MTT., vol. 34, No.6, pp. 660-665, Jan., 1986.

Djo87 A. R. Djordjevic, T. K. Sarkar, and R. F. Harrington, "Time-Domain Response of Multiconductor Transmission Lines," Proceedings of IEEE, vol. 75, No.6, pp. 743-764, Jun., 1987.

Djo89a A. R. Djordjevic, R. F. Harrington, T. K. Sarkar, and M. Bazdar, Matrix Parameters for Multiconductor Transmission Lines: Software and User's Manual, Artech House. Inc., Norwood, MA, 1989.

Djo89b A. R. Djordjevic, R. F. Harrington, T. K. Sarkar, and M. Bazdar, Time-Domain Response of Multiconductor Transmission Lines: Software and User's Manual, Artech House. Inc., MA, 1989.

Dwo79 L. N. Dworsky, Modern Transmission Line Theory and Applications, John Wiley & Sons, Inc. New York, NY, pp. 46-51, 1979.

EEs86 TOUCHSTONE User's Manual, Version 1.32, EEsof. Inc., Westlake Village, CA, Aug., 1986.

Eis92 W. R. Eisenstadt and Y. Eo, "S-Parameter-Based IC Interconnect Transmission Line Characterization," IEEE Trans. CHMT., vol. 15, No.5, pp. 483-490, Aug., 1992.

Eo90 Y. Eo and W. R. Eisenstadt, "IC Interconnect Capacitance and Conductance Determination," SRC TECHON 90, San Jose, CA, Oct., 16-18, 1990.

Eo92a Y. Eo and W. R. Eisenstadt, "High Speed VLSI Interconnect Modeling Based on S-Parameter Measurements," submitted on IEEE Trans. CHMT.

Eo92b Yungseon Eo, and W. R. Eisenstadt, "SPAIL (Scattering Parameter Analysis of Interconnect Lines) User's Manual," Dept. of Electrical Eng., University of Florida, Gainesville FL, 1992.

Fit78 Jim Fitzpatrick, "Error Models for System Measurements," Microwave Journal, Vol., pp. 63-66, May, 1978.

Fra77 Sidney Frankel, Multiconductor Transmission Line Analysis, Artech House Inc., Norwood, MA, 1977.

Gra84 Paul R. Gray and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, Inc, New York, 1984.

Get73 William J. Getsinger, " Microstrip Dispersion Model," IEEE Trans. MTT., vol. MTT-21, No.1, 34-39, Jan., 1973.

Ghi89 G. Ghione, I. Maio, and G. Vecchi, "Modeling of Multiconductor Buses and Analysis of Crosstalk, Propagation Delay and Pulse Distortion in High-Speed GaAs Logic Circuits," IEEE Trans. MTT., vol. 37, No.3, pp. 445-456, Mar., 1989.

Goo89 K. W. Goosen and R. B. Hamond, "Modeling of Picosecond Pulse Propagation in Microstrip Interconnections on Integrated Circuits," IEEE Trans. MTT., vol. 37, No.3, pp. 469-478, Mar., 1989.

Gup79 K.C. Gupta, R. Grag, and I. J. Bahl, Microstrip Lines and Slotlines., Artech House Inc., Dedham, MA, 1979.

Gup81 K.C. Gupta, R. Grag, and R. Chadha, Computer Aided Design of Microwave Circuits., Artech House Inc., Dedham, MA, 1981.

Has71 H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of Microstrip Lines on Si-SiO_2 System," IEEE Trans. Microwave Theory Tech., vol. MTT-19, pp. 869-881, Nov., 1971.

Has84 H. Hasegawa, Shouhei Seki, "Analysis of Interconnection Delay on Very High-Speed LSI/VLSI Chips Using an MIS

Microstrip Line Model," IEEE Trans. Electron Devices, vol. ED-31, No. 12, pp. 1954-1960, Dec., 1984.

Hat87 M. Hatamian, L. A. Hornak, T. E. Little, S. K. Tewksbury, and P. Franzon, "Fundamental Interconnect Issues," AT&T Technical Journal, vol.66, Issue 4, pp. 13-30, Jul., 1987.

Hp85 HP8510 Network Analyzer System Operating and Programming Manual, Hewlett Packard Corp., Santa Rosa, CA, Jan., 1985.

Hp90 HP 54121T Digitizing Oscilloscope, Hewlett Packard Company, Santa Rosa, CA, 1990.

Hol90 Albert L. Holloway, "Analysis and Design of Generalized Microstrip," Ph.D. Dissertation, University of Florida, Gainesville, 1990.

Hwa91 L. T. Hwang, D. Nayak, I. Turlik, and A. Reisman, "Thin-Film Pulse Propagation Analysis Using Frequency Techniques," IEEE Trans. CHMT., vol. 14, pp. 192-198, No.1, Mar., 1991.

Ika82 Y. Ikawa, W. R. Eisenstadt, and R. W. Dutton, "Modeling of High-Speed, Large-Signal Transistor Switching Transients from S-Parameter Measurements," IEEE Trans. ED., vol. ED-29, No.4, pp. 669-675, Apr., 1982.

Isa73 J. C. Isaacs, JR. and N. A. Strakhov, "Crosstalk in Uniformly Coupled Lossy Transmission Line," Bell Syst. Tech. J., vol. 52, No.1, pp. 101-115, Jan., 1973.

Kau89 H. R. Kaupp, "Waveform Degradation in VLSI Interconnections," IEEE Journal of Solid-State Circuits, vol. 24, No.4, pp. 1150-1153, Aug., 1889.

Lin90a Mou-Shiung Lin, "Measured Capacitance Coefficients of Multiconductor Microstrip Lines with Small Dimensions," IEEE Trans. CHMT., vol.13, No.4, pp. 1050-1990, Dec., 1990.

Lin90b M. S. Lin, A. H. Engvik, and J. S. Loos, "Measurements of Transient Response on Lossy Microstrip with Small Dimensions," IEEE Trans. CAS., vol.37. No 11, pp. 1383-1393, Nov., 1990.

Lio90 J. C. Liao, O. A. Plansinski, and J. L. Prince, "Computation of Transients in Lossy VLSI Packaging Interconnections," IEEE Trans. CHMT., vol. 13, No.4, pp. 833-838, Dec., 1990.

Liz92 Elvira B. Liz, "Development and Characterization of Planar Spiral Inductors on Silicon Substrates," Master's Thesis, University of Florida, Dec., 1992.

Mat69 Richard E. Matick, Transmission Lines for Digital and Communication Networks, McGraw-Hill Inc., New York, 1969.

Met91 HSPICE User's Manual H9001, Meta Software, Cupertino, CA, 1991.

Nay89 D. Nayak, L-T. Hwang, and I. Turlik, "Calculation of Electrical Parameters of a Thin-Film Multichip; Package," IEEE Trans. CHMT., vol. 12, No.2, pp. 303-369, Jun., 1989.

Pin85 M. R. Pinto, C. S. Rafferty, H. R. Yeager., and R. W. Dutton, "PISCES-II Technical Report," Stanford Electronics Laboratories, Dept. Electrical Eng., Stanford University, Stanford CA, 1985.

Pra83 P. Pramanick and P. Bhartia, "An Accurate Description of Microstrip," Microwave J., vol. 26, pp. 89-93, Dec., 1983.

Puc68 R. A. Pucel, D. J. Masse, and C. P. Hartwig, "Losses in Microstrip," IEEE Trans. MTT, vol. MTT-16, No.6, pp. 342-350, June 1968.

Ram65 Simon Ramo, John R. Whinnery, and Theodore Van Duzer, Fields and Waves in Communication Electronics, Wiley and Sons Inc., New York, 1969.

Rue75 Albert E. Ruehli and Pierce A. Brennan, "Capacitance Models for Integrated Circuit Metalization Wires," IEEE J. of Solid-State Circuit, vol. SC-10, No.6, pp. 530-536, Dec., 1975.

Sac90 Krzystof Sachse, "The Scattering Parameters and Directional Coupler Analysis of Characteristically Terminated Asymmetric Coupled Transmission Lines in an Inhomogeneous Medium," IEEE Trans MTT., vol. 38, No.4, pp. 417-425, Apr., 1990.

Sak83 T. Sakurai and K. Tamaru, "Simple Formula for Two- and Three-Dimensional Capacitances," IEEE Trans. Electron Device, vol. ED-30, No.2, pp. 183-185, Feb., 1983.

Sax92 Arjun N. Saxena, "Interconnect for the '90s: Alumimum-Based Multilevel Interconnects and Future Directions," IEDM 1992 Short Course: Interconnect for the '90s, San Jose, CA, 1992.

Sch69 M. V. Schneider, "Microstrip Lines for Microwave Integrated Circuits," Bell Syst. Tech. J., vol. 48, pp. 1421-1443, 1969.

Sch89 Jose E. Schutt-Aine and Raj Mittra, "Nonlinear Transient Analysis of Coupled Transmission Lines," IEEE Trans. CAS., vol. 36, No.7, pp. 959-966, Jul., 1989.

Sek84 Shouhei Seki and H. Hasegawa, "Analysis of Crosstalk in Very High-Speed LSI/VLSI's Using a Coupled Multiconductor MIS Microstrip Model," IEEE Trans. Microwave Theory Tech., vol. MTT-32, pp. 1715-1720, Dec., 1984.

Tma90 TMA PISCES-IIB, Two-Dimensional Device Analysis Program, version 9033, Technology Modeling Associations Inc., Palo Alto, CA, Nov.15, 1990.

Tri90 V. K. Tripathi, J. B. Rettig, and L. Hayden, "Characterization of Multiple Coupled Interconnection Lines from Time Domain Measurements," IEEE Proceedings of the 1990 VMIC, Santa Clara, CA pp. 416-418, 1990.

Ush90 Uukihiro Ushiku, Hidefumi Kushibe, Hisako Ono "Design Guidelines for Deep-Sub-Micrometer Interconnections," IEEE Proceedings of the 1990 VMIC, pp. 413-415, 1990.

Yam68 Eikichi Yamashita, "Variational Method for the Analysis of Microstrip-like Transmission Lines," IEEE Trans. MTT, vol. MTT-16, No.8, pp. 529-535, Aug., 1968.

You90 H. You and M. Soma, "Crosstalk Analysis of Interconnect Lines and Packages in High Speed Integrated Circuits," IEEE Trans. CAS., vol. 37, No.8, pp. 1019-1026, Aug., 1990.

Yua83 C. P. Yuan, "Modeling and Extraction of Interconnect Parameters in VLSI Circuits," Ph.D. Dissertation, University of Illinois, Urbana Champaign, 1983.

Yua82a C. P. Yuan and T. N. Trick, "A Simple Formula for the Estimation of the Capacitance of Two-dimensional Interconnects in VLSI Circuits," IEEE Electron Device Letter vol. EDL-3, No.12, pp. 391-393, Dec., 1982.

Yua82b H. T. Yuan, et al, "Properties of Interconnection on Silicon, Sapphire, and Semi-Insulating Gallium Arsenide," IEEE Trans. Electron Devices, vol. ED-29, No.4, pp. 639-644, Apr., 1982.

Yua91 J. S. Yuan and W. R. Eisenstadt, "A Novel Lossy and Dispersive Interconnect Model for Integrated Circuit

Simulation," IEEE Trans. CHMT, vol. 15 No.2, pp. 275-280, Jun., 1991.

Veg86 Richard L. Veghte and Constantine A. Balanis, "Dispersion of Transient Signals in Microstrip Transmission Lines," IEEE Trans. MTT., vol. MTT-34, No.12, pp. 1427-1436, Dec., 1986.

Wee70 William T. Weeks, "Calculation of Coefficients of Capacitance of Multiconductor Transmission Lines in the Presence of a Dielectric Interface," IEEE Trans. MTT., vol. MTT-18, No.1, pp. 35-43, Jan., 1970.

Wei84 Cao Wei, et al, "Multiconductor Transmission Lines in Multilayered Dielectric Media," IEEE Trans. MTT., vol. 32, No.4, pp. 439-450, Apr., 1984.

Whe42 A. Wheeler, "Formulas for the Skin Effects," Pro. IRE, pp. 412-424, 1942.

Whe77 H. A. Wheeler, "Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane," IEEE Trans. MTT, vol. MTT-25 No.8, pp. 631-647, Aug., 1977.

Whi87 John F. Whitaker, Theodore B. Norris, G. Mourou, and Tomas Y. Hsiang, "Pulse Dispersion and Shaping in Microstrip Lines," IEEE Trans. MTT., vol. MTT-35, No.1, pp. 41-47, Jan., 1987.

Wij87 P. J. Van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A New Straightforward Calibration and Correction Procedure for "on wafer" High Frequency S-Parameter Measurements (45MHz-18GHz)," IEEE Proceedings of the 1987 BCTM, pp. 70-73, 1987.

Win91 D. Winklestein, M. B. Steer and R. Pomerleau, "Simulation of Arbitrary Transmission Line Networks with Nonlinear Terminations," IEEE Trans. CAS., vol. 38, No.4, pp. 418-422, Apr., 1991.

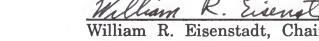
BIOGRAPHICAL SKETCH

Yungseon Eo was born in Kyung-gi-do, Korea, on October 25, 1960. He received his B.S. and M.S. degrees in electronic engineering from Hanyang University, Seoul, Korea, in 1983, and 1985, respectively. Since August 1988, he has been working toward the Ph.D. degree in electrical engineering at the University of Florida, Gainesville, FL.

From 1986 to 1988, he worked at Korea Telecommunication Authority Research Center, Seoul, Korea, where he performed telecommunication network planning and software design.

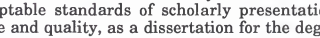
His current research interests are high frequency integrated circuit device measurement, modeling, and simulation related to high speed VLSI circuit design, advanced packaging, and microwave integrated circuit design.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



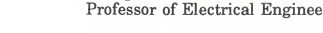
William R. Eisenstadt, Chairman
Associate Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



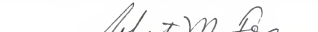
Sheng S. Li
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



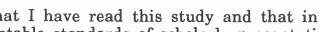
Robert M. Fox
Associate Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Mark E. Law
Assistant Professor of Electrical Engineering

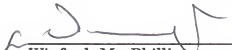
I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Joseph N. Wilson
Assistant Professor of Computer and Information Sciences

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1993



Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School